

Layout Note:
Comp0,2 connect with Z0=27.4 ohm, make trace length shorter than 0.5".
Comp1,3 connect with Z0=54.9 ohm, make trace length shorter than 0.5".

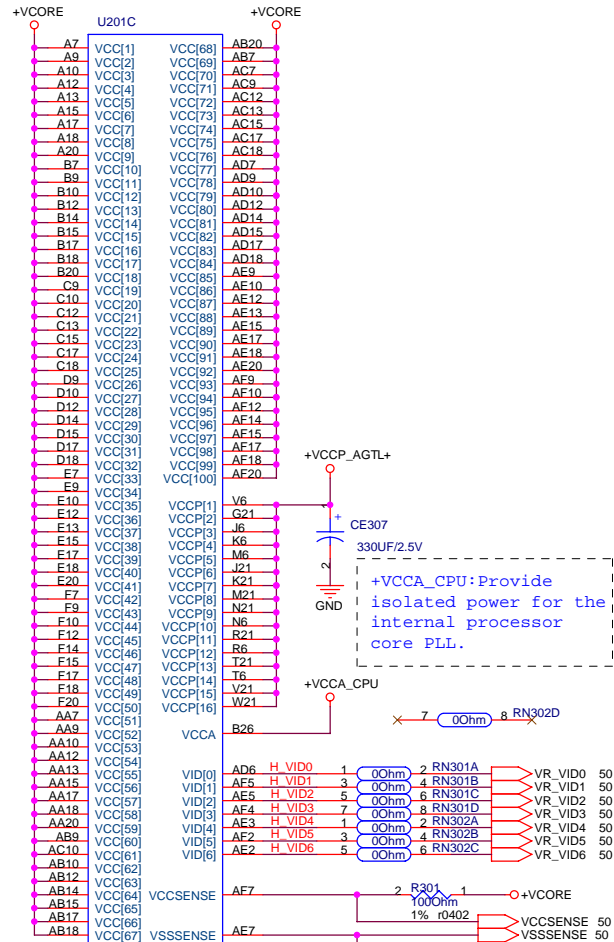
PROCHOT# is not supported
S/W doesn't define it yet.

H_CPURST# 1
H_ADS# 1

<Variant Name>

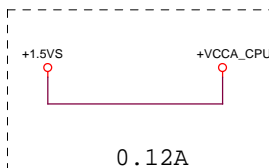
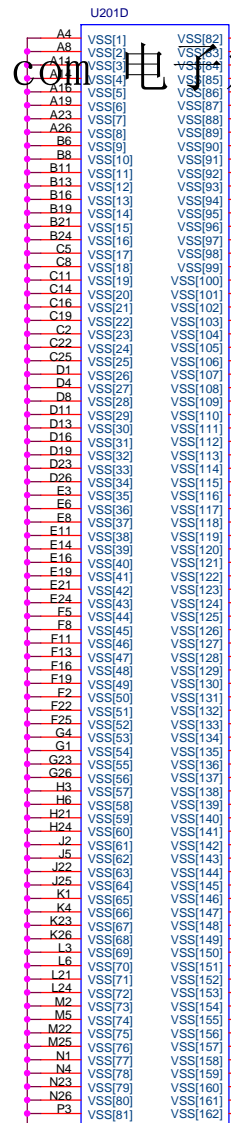
YUNAH FSB667	LFM	TYP	HFM
VCC	1.14V	1.2V	1.356V
C4	0.3	0.3	0.3
ICC	0.9A	1.55A	2.7A

YUNAH FSB667	Min	Typ	Max
VCCP	0.997V	1.05V	1.102V
C4	0.3	0.3	0.3
ICC	0.9A	1.55A	2.7A

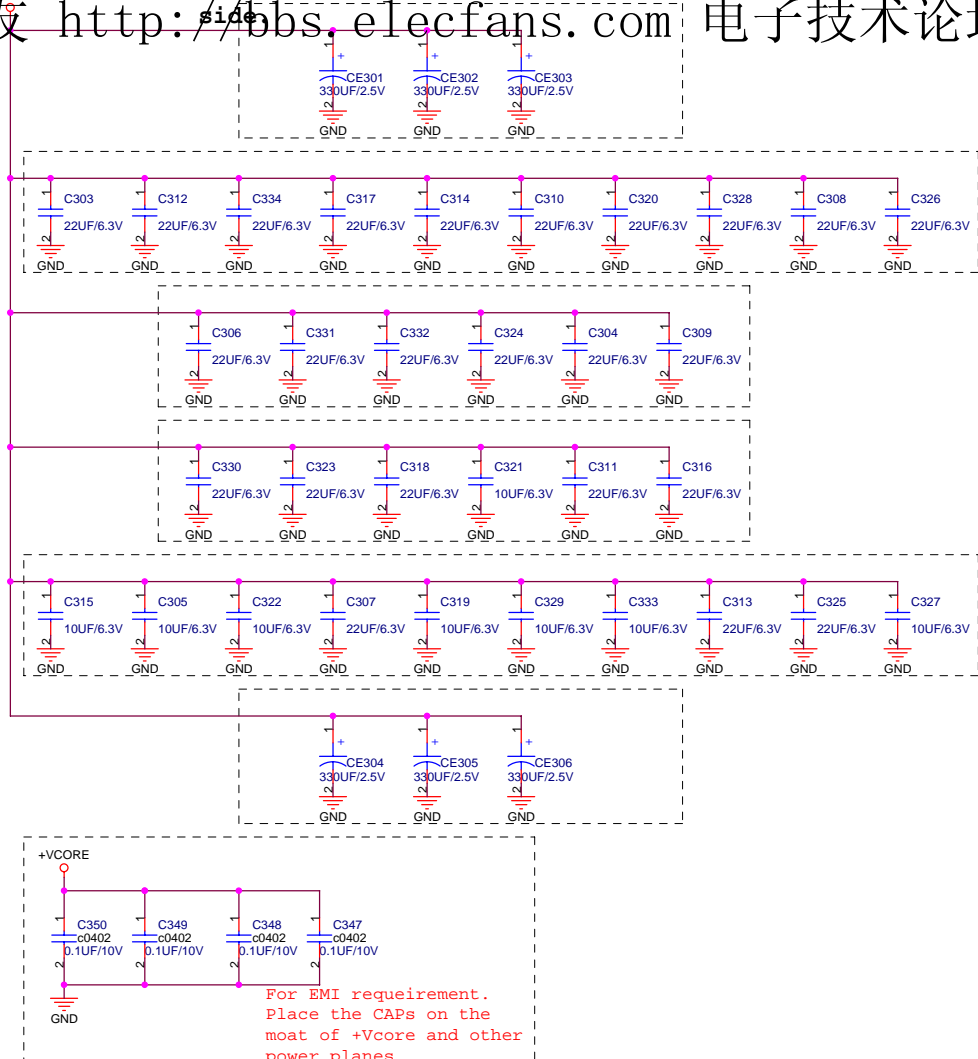


Layout note: Route VCCSENSE and VSSSENSE trace at 27.4 ohm with 25 mils spacing mismatch and 18mils trace on 7mils spacing.

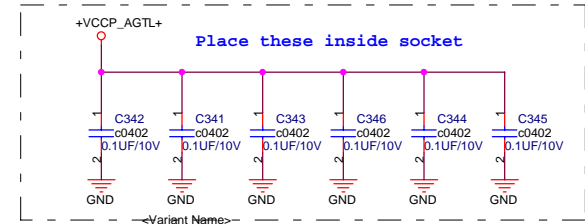
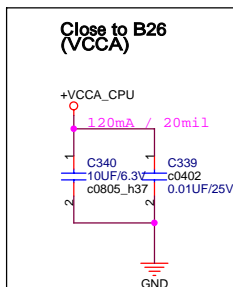
Place pull-up/down resistors within 1 inch of CPU.



Vcc Core Decoupling Caps
Place these on bottom side



For EMI requirement. Place the CAPS on the moat of +Vcore and other power planes



ASUS		Title : Yonah CPU (2)	
ASUSTek COMPUTER INC		Engineer: Charles Lee	
Size	Project Name	Rev	
Custom	A6Jc	2.1	
Date: Thursday, January 19, 2006		Sheet 3 of 63	

Fan Speed Control

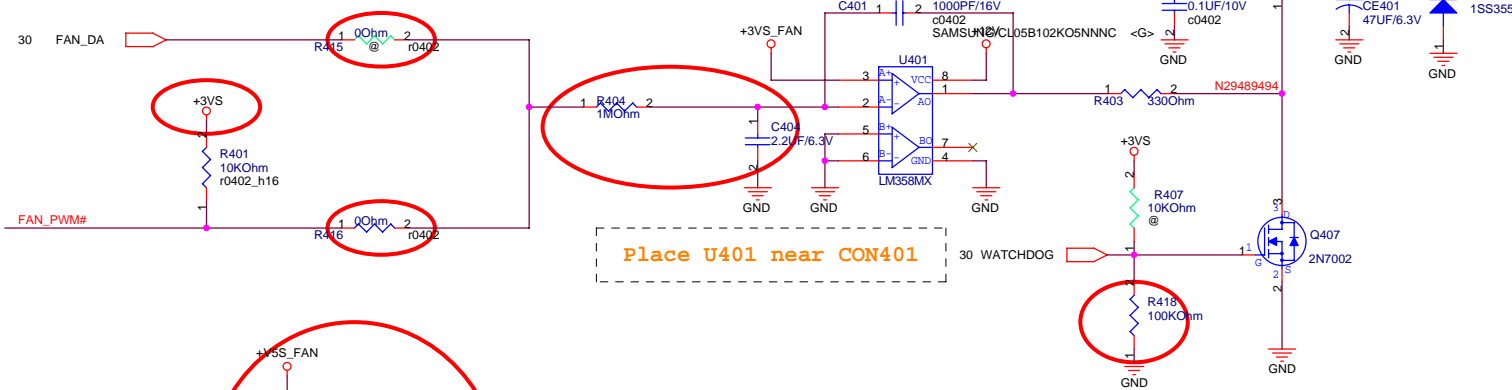
<http://www.elecfans.com>

电子发烧友

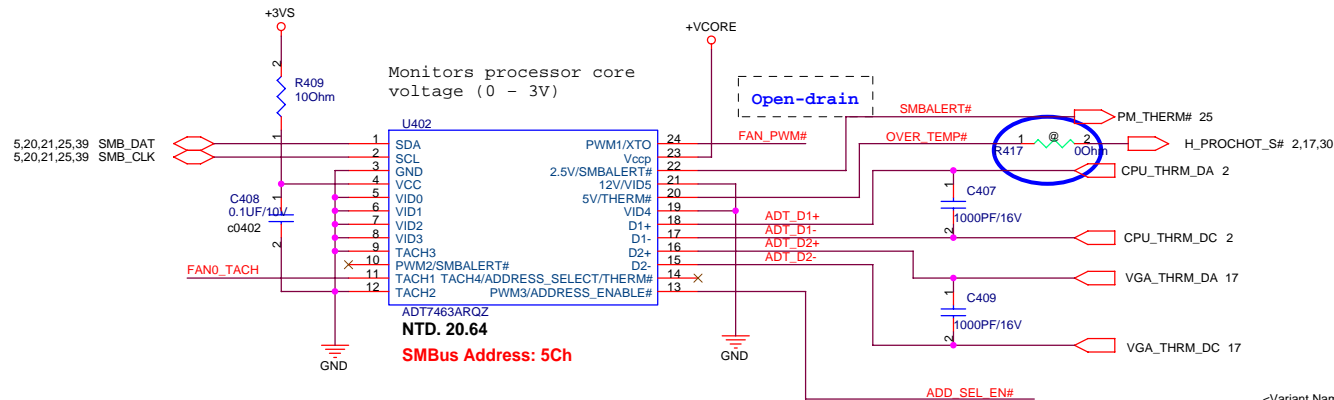
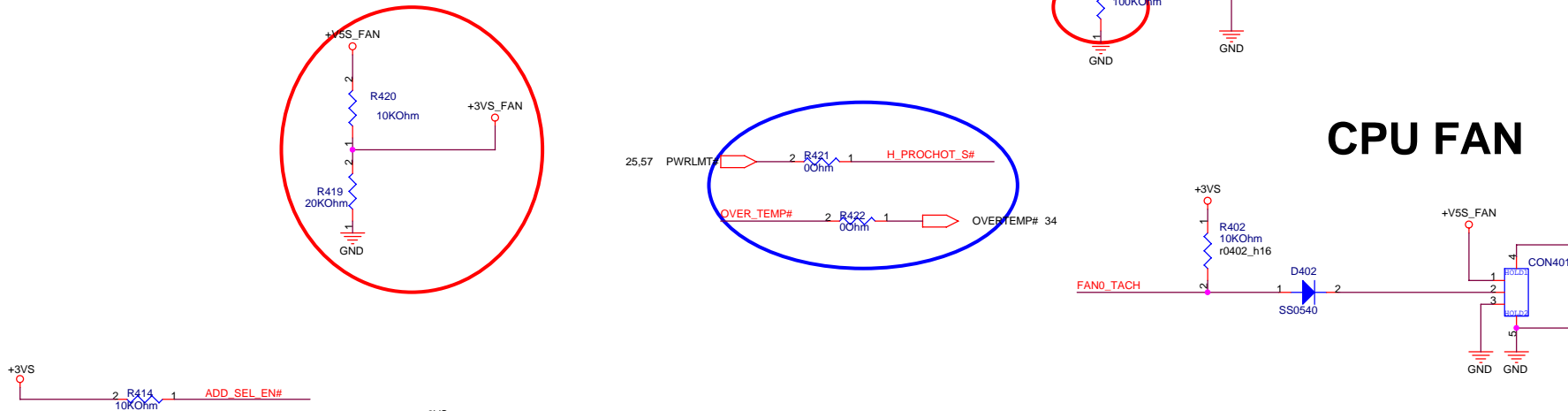
Using a OP AMP and fine-tuning the level, we can improve the fan speed accuracy.

<http://bbs.elecfans.com>

电子技术论坛



CPU FAN



Route H_THERMDA and H_THERMDC on the same layer

OTHER SIGNALS

12 mils

=====GND

10 mils

=====H_THERMDA(10 mils)

10 mils

=====H_THERMDC(10 mils)

10 mils

=====GND

12 mils

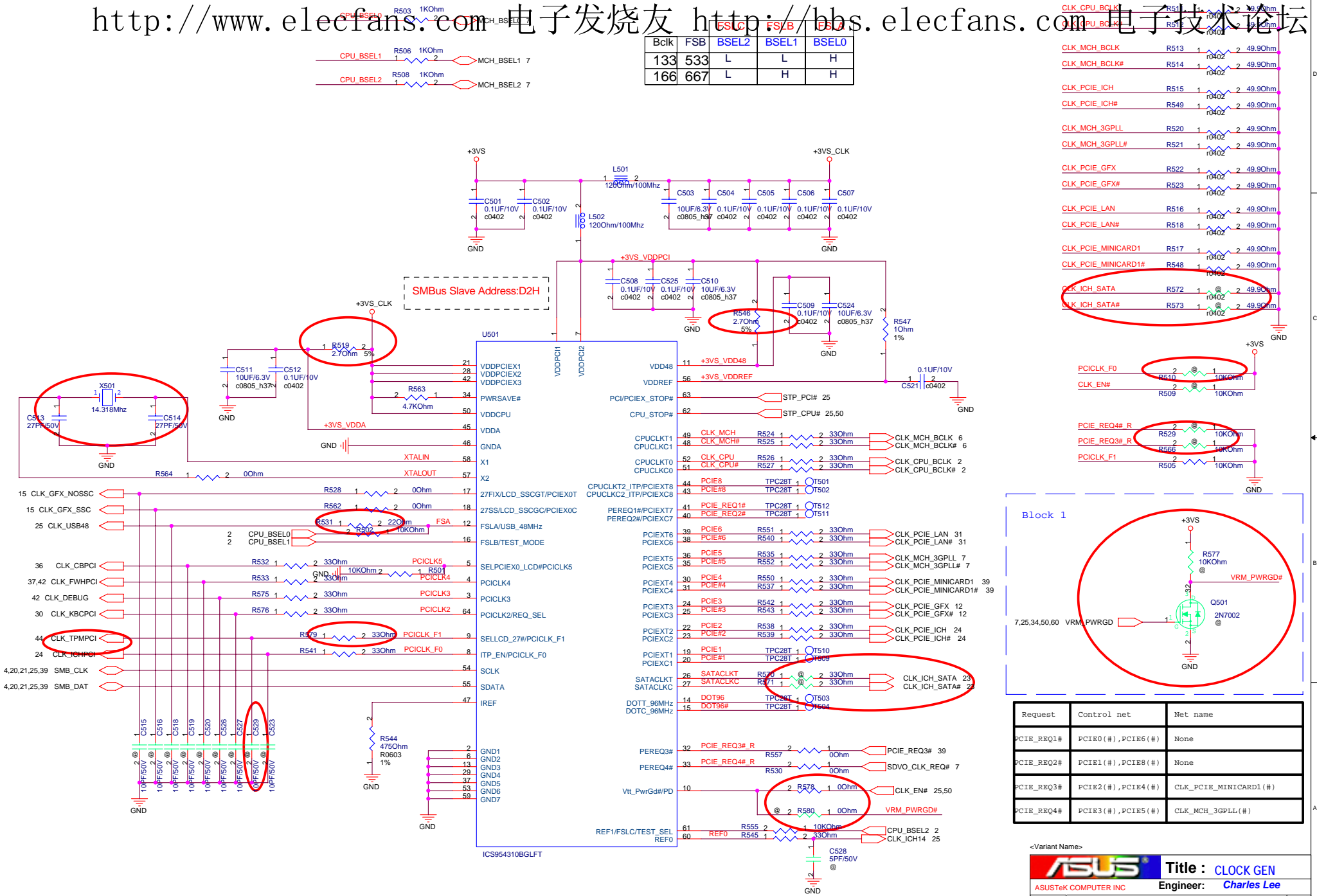
OTHER SIGNALS

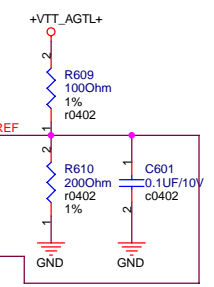
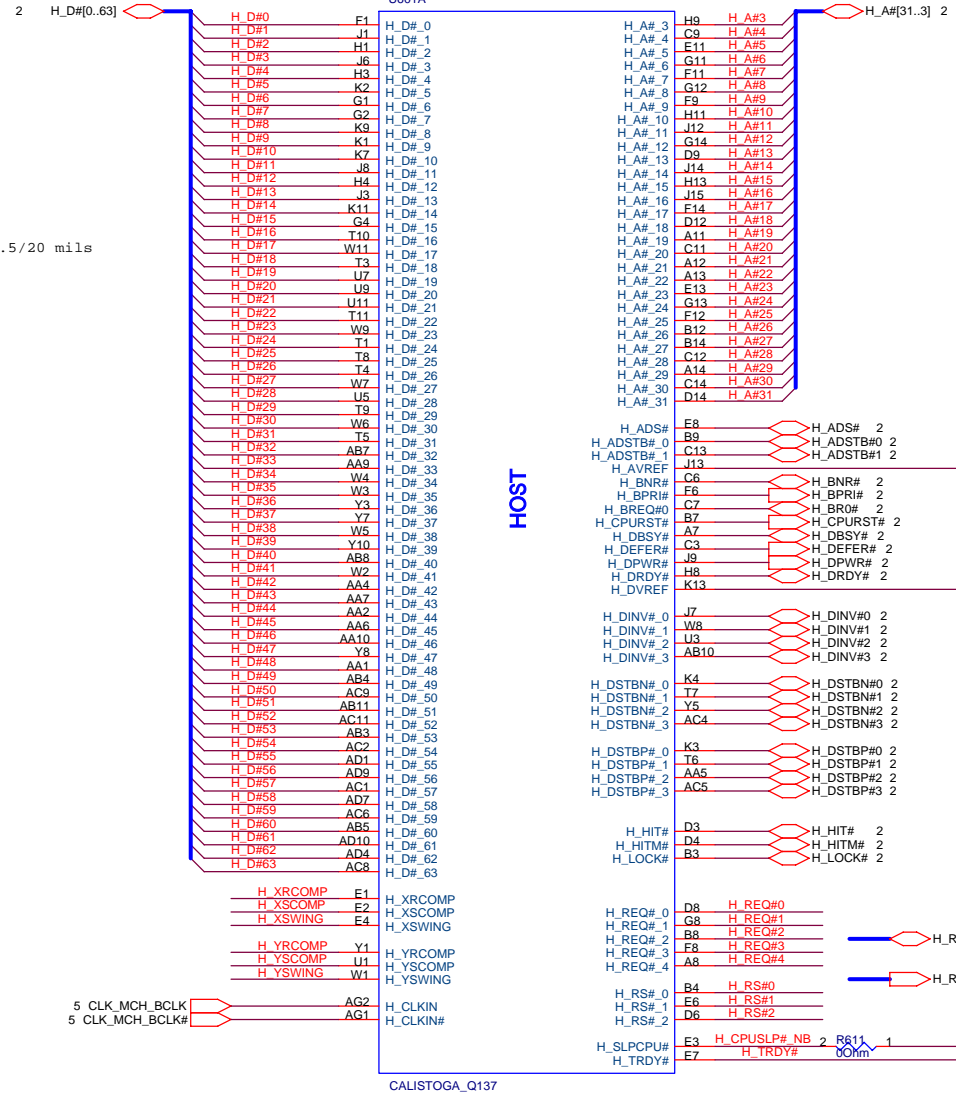
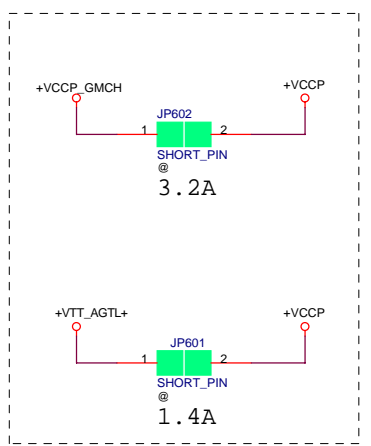
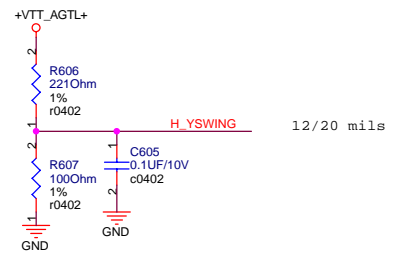
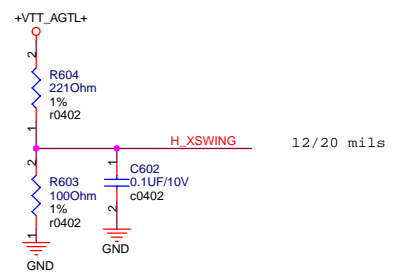
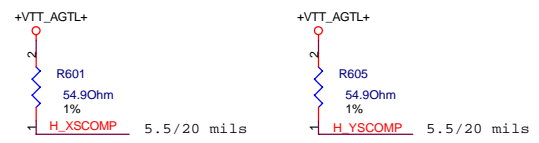
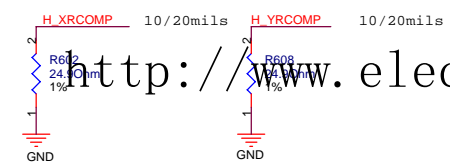
Avoid BPSB,Power

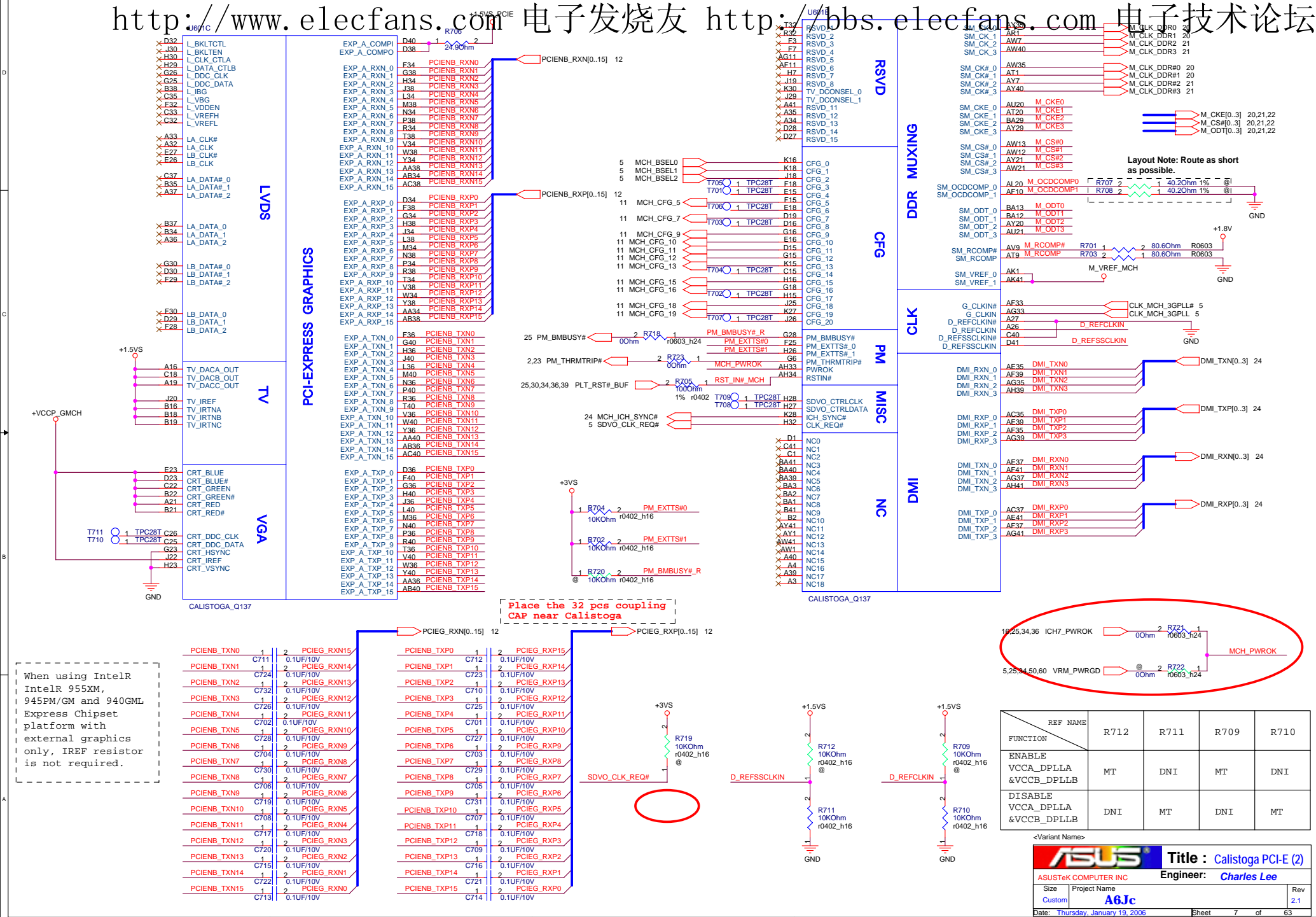
ASUS		Title : THER-SENSOR,FAN	
ASUSTeK COMPUTER INC		Engineer: Marco Chen	
Size	Project Name	Rev	
Custom	A6Jc	2.1	
Date: Thursday, January 19, 2006		Sheet	4 of 63

Place termination closed to source IC

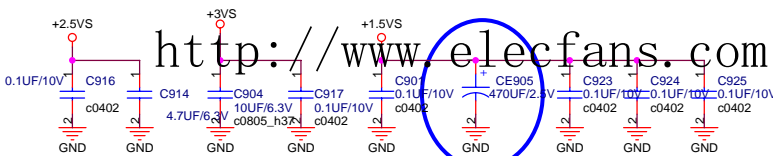
Bclk	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H





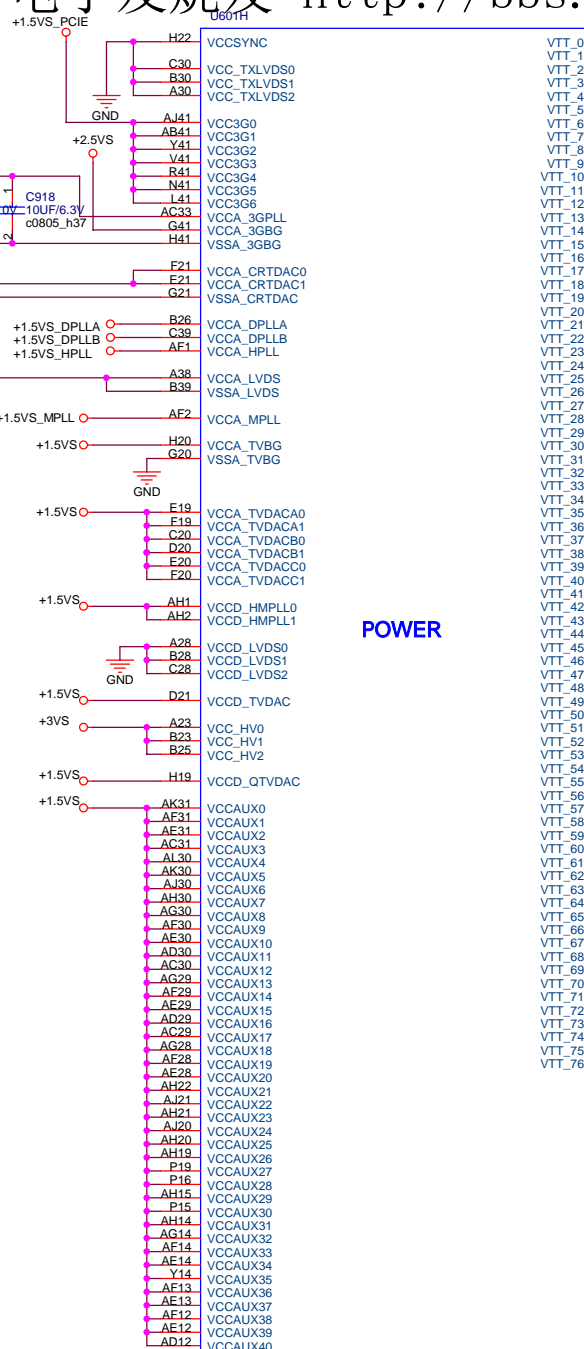
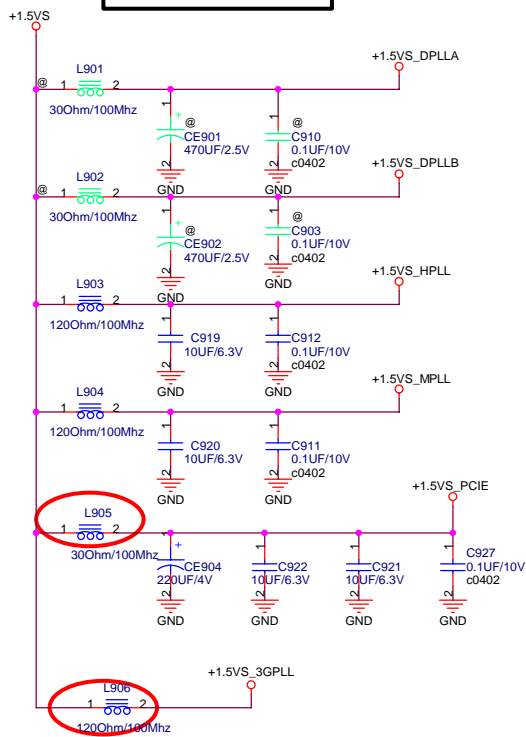




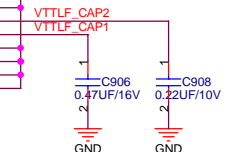
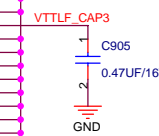
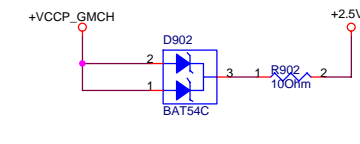
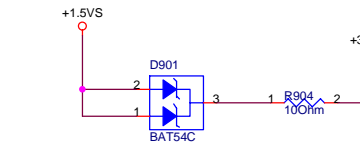
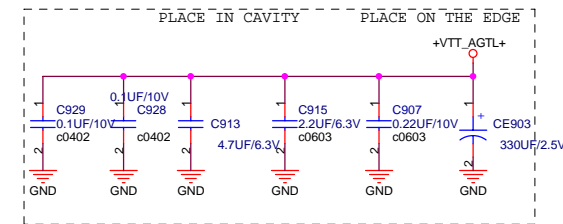


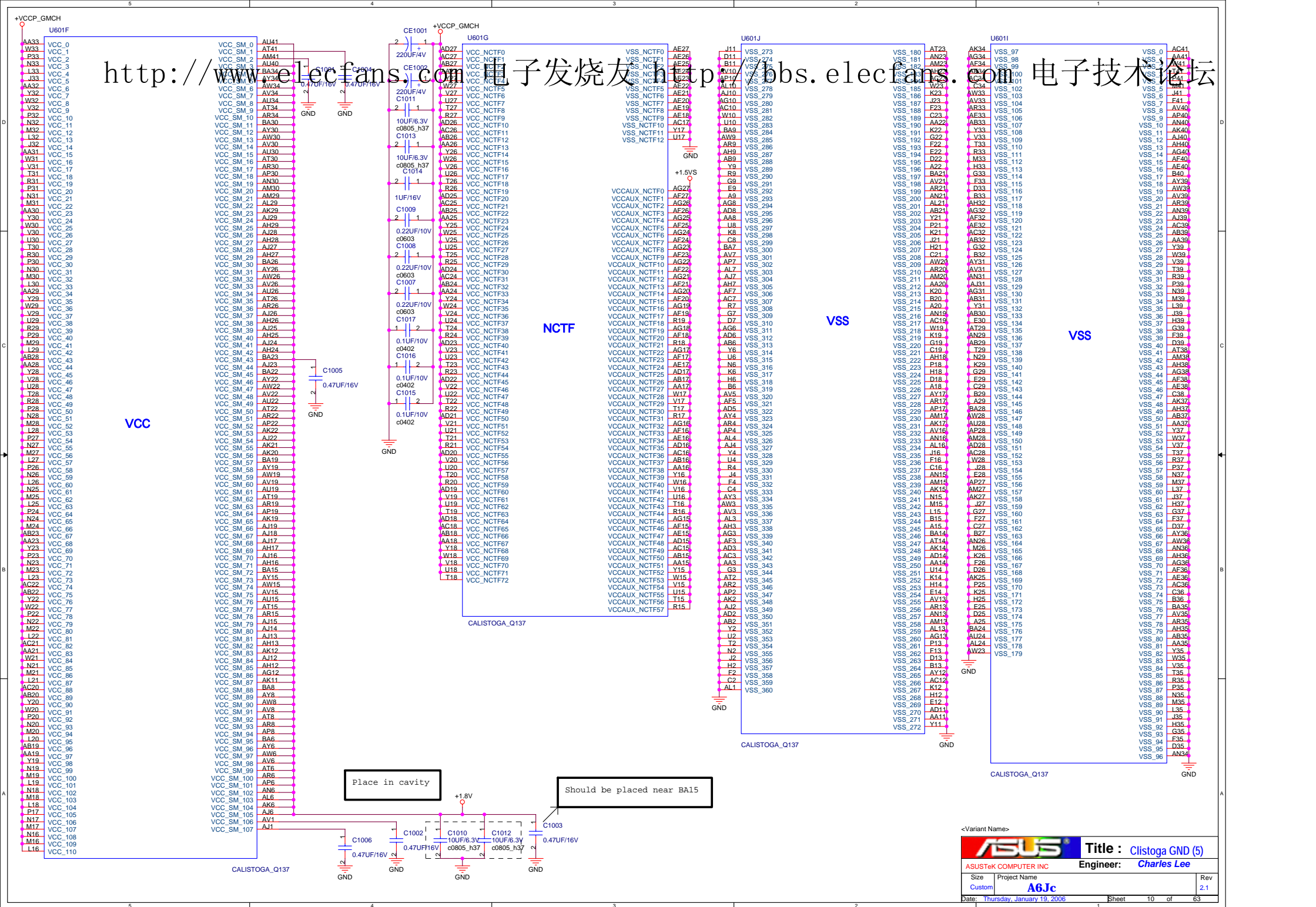
NOTE: 0.1uF CAPS USED IN
+1.5VS, +3.3VS
+2.5VS should be placed within
200 mils of edge.

NOTE: 0.1uF caps in
1.5VS_XPLL need to be
located as edge caps
within 200 mils.



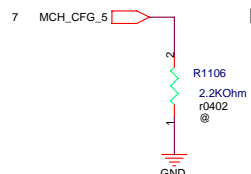
POWER





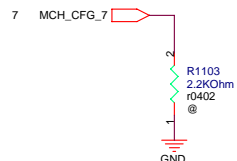
CFG5 : DMI STRAP

LOW = DMI X 2
HIGH = DMI X 4 (Default)



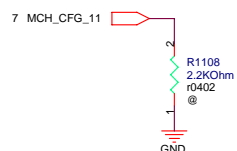
CFG7 : CPU STRAP

LOW = Mobile Prescott
HIGH = Dothan CPU (Default)



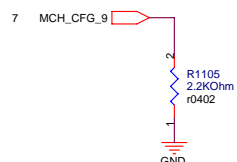
CFG11 : PSB 4X CLK ENABLE

LOW = REVERSAL
HIGH = Calistoga (Default)



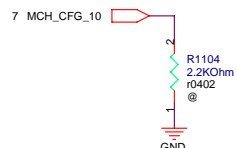
CFG9 : PCIE GRAPHIC LANE

LOW = REVERSE LANE (Default)
HIGH = NORMAL OPERATION



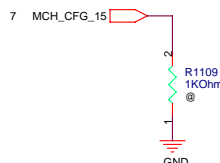
CFG10: HOST PLL VCO SELECT

LOW = RESERVED
HIGH = MOBILITY



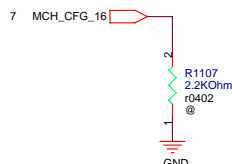
CFG15 : ICH RESET DISABLE

LOW = ICH RESET DISABLE
HIGH = NORMAL OPERATION



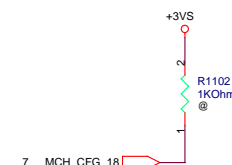
CFG16 : FSB DYNAMIC ODT

LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)



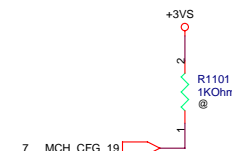
CFG18 : GMCH Core Voltage Level

LOW = 1.05V (Default)
HIGH = 1.5V



CFG19 : DMI LANE REVERSAL

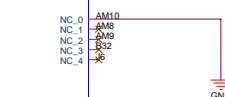
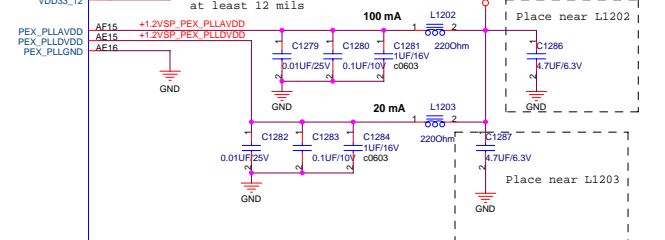
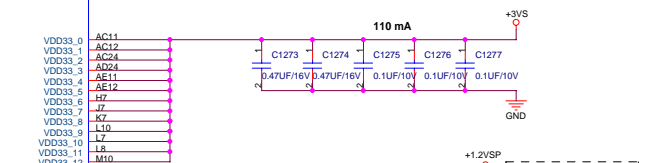
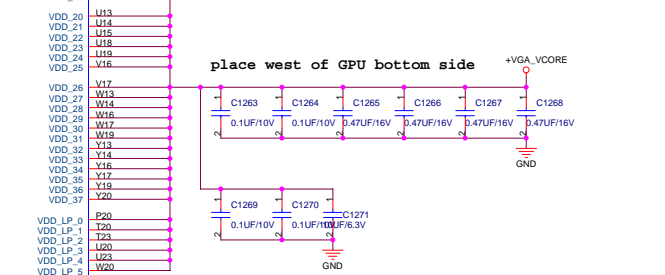
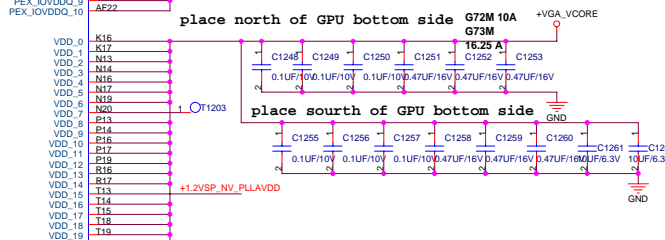
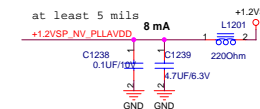
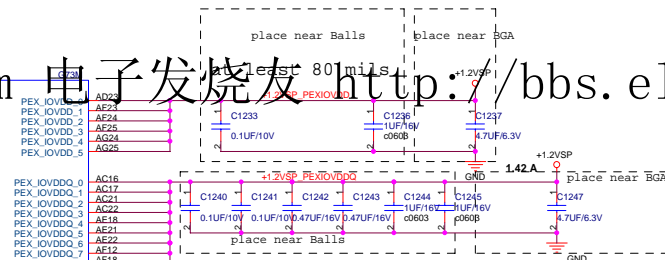
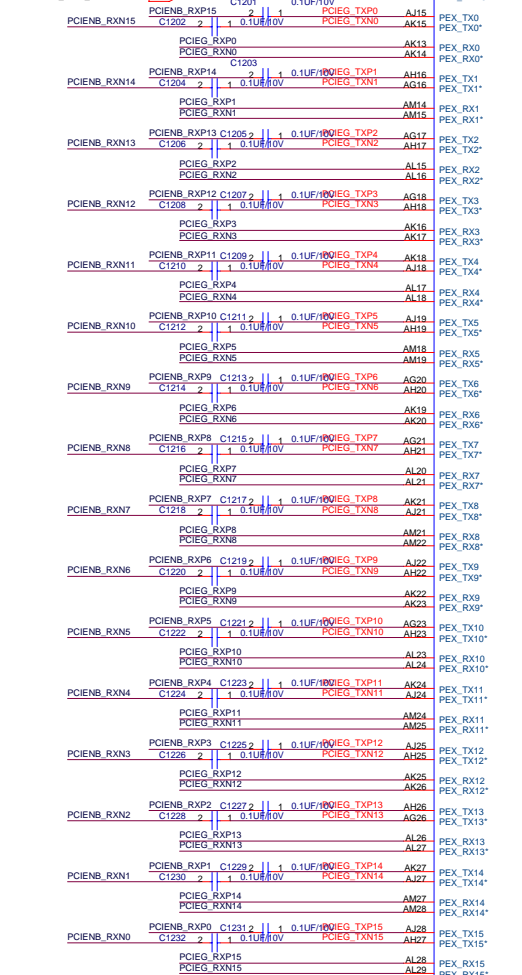
LOW = NORMAL
HIGH = LANES REVERSED

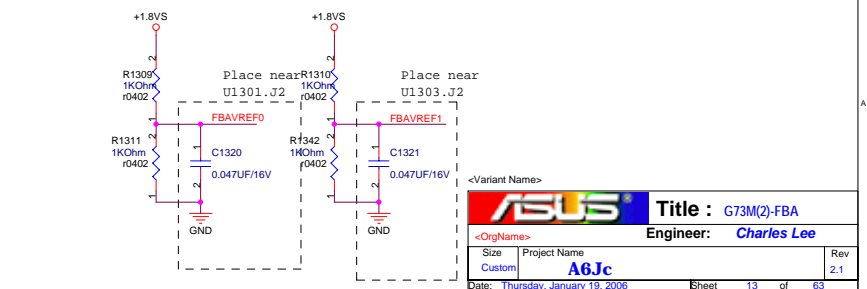
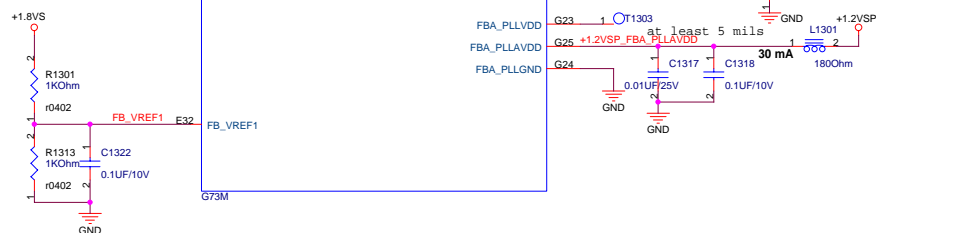
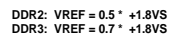
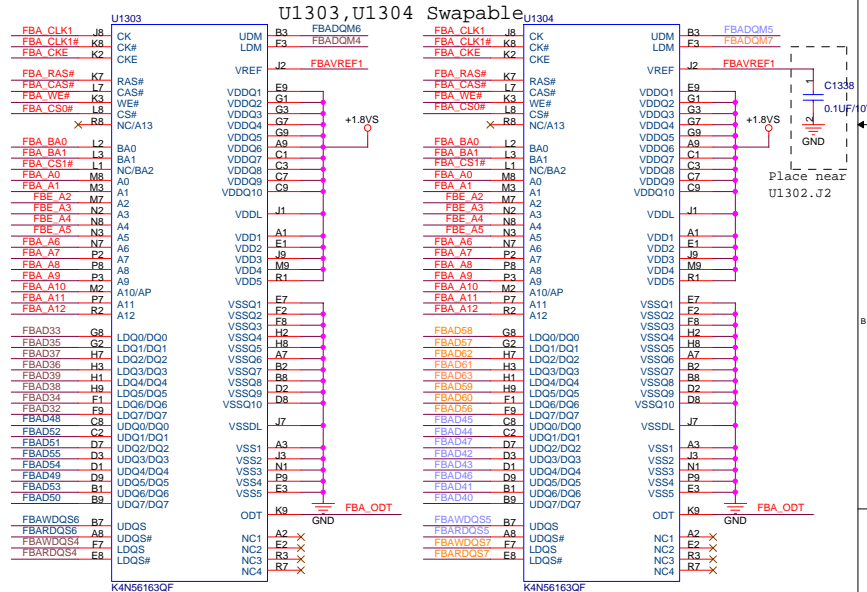
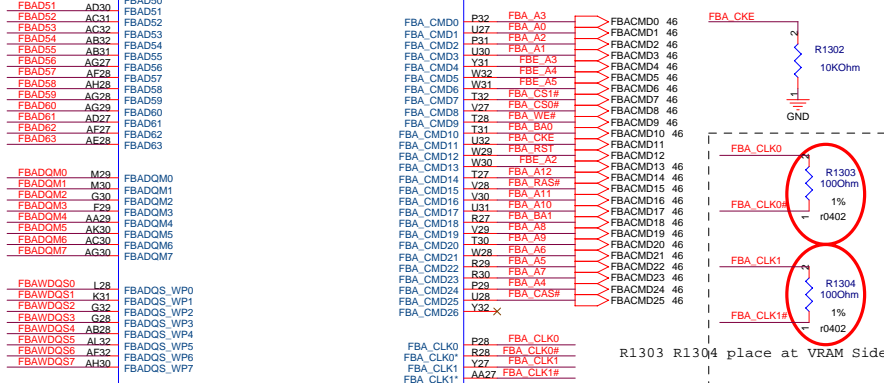
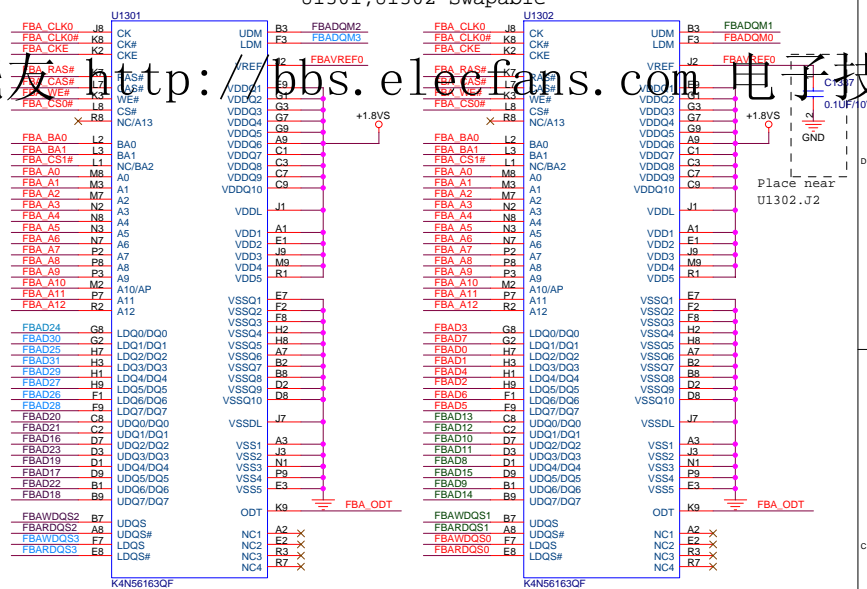
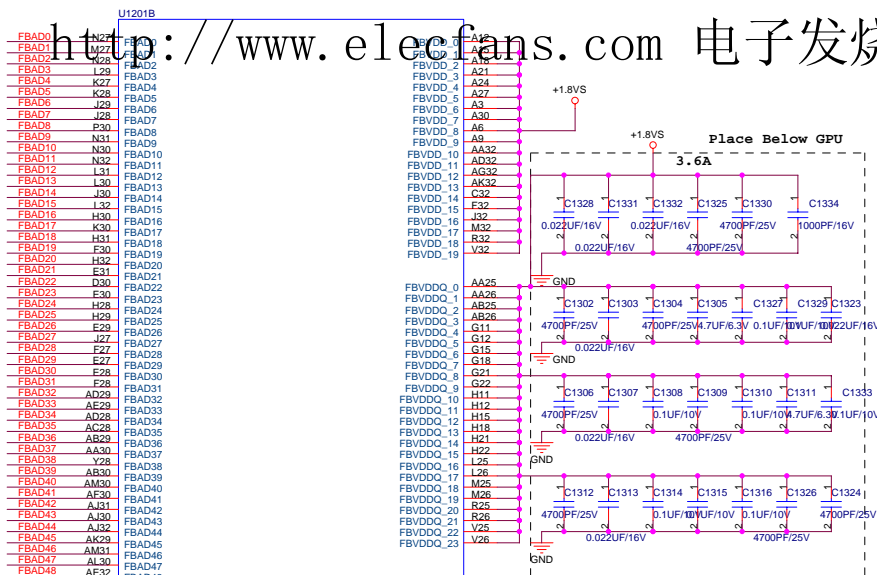


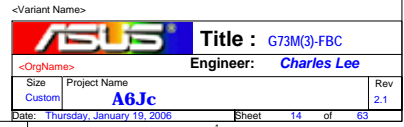
CFG[17..3] have internal pullup resistors.
CFG[15..18] have internal pulldown resistors.
SDVOCRTL_DATA has internal pulldown resistors.

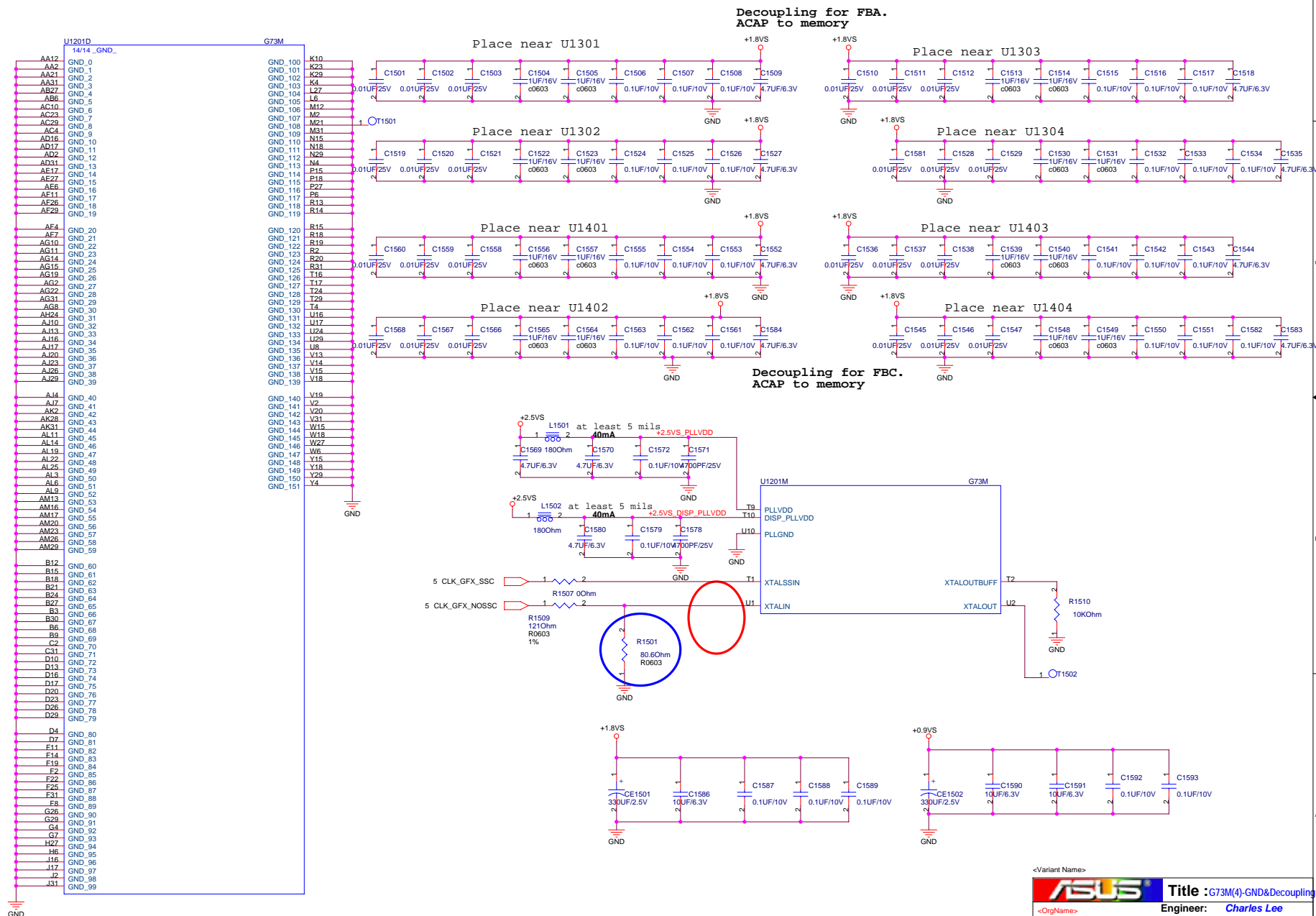
<Variant Name>

		Title : Calistoga Strapping	
ASUSTeK COMPUTER INC		Engineer: Charles Lee	
Size	Project Name	Rev	
Custom	A6Jc	2.1	
Date: Thursday, January 19, 2006		Sheet	11 of 63









<Variant Name>

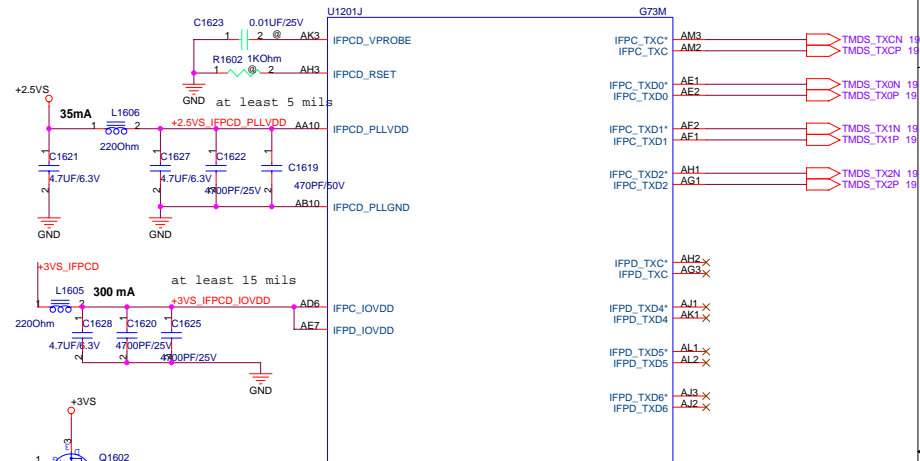
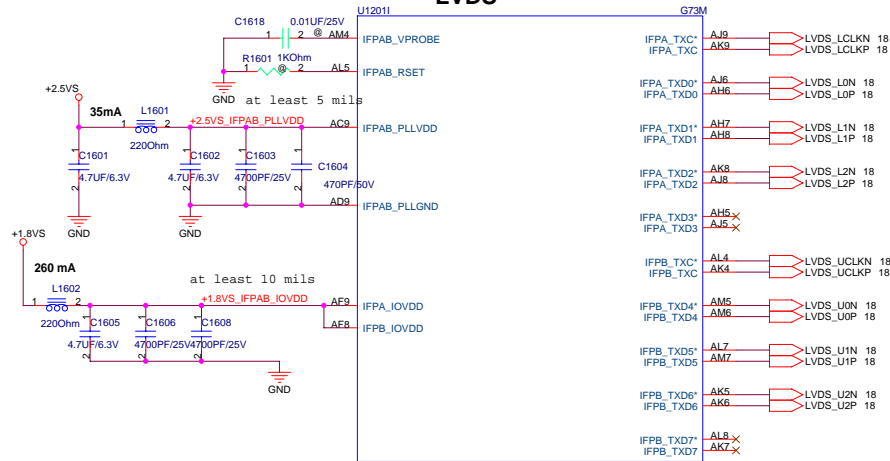
ASUS Title : G73M(4)-GND&Decoupling

Engineer: Charles Lee

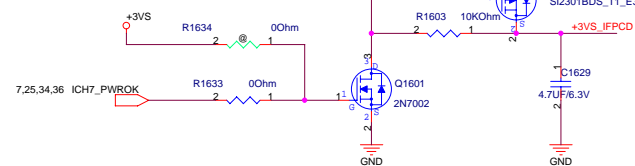
Size Project Name Rev
Custom A6Jc 2.1

Date: Thursday, January 19, 2006 Sheet 15 of 63

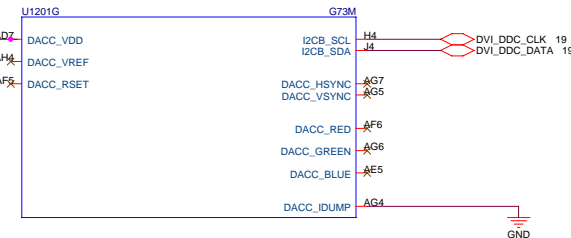
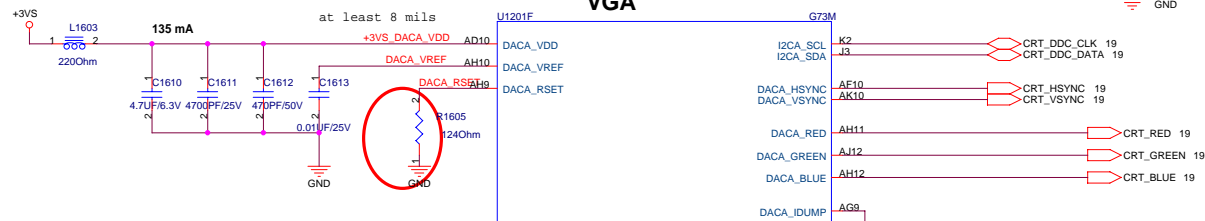
LVDS



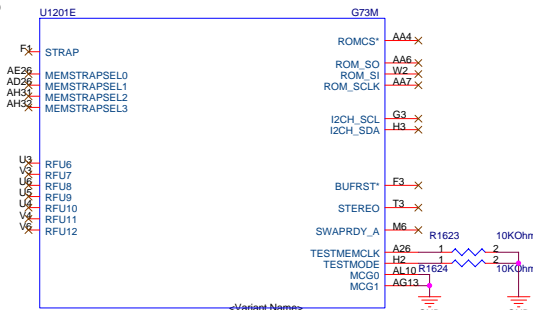
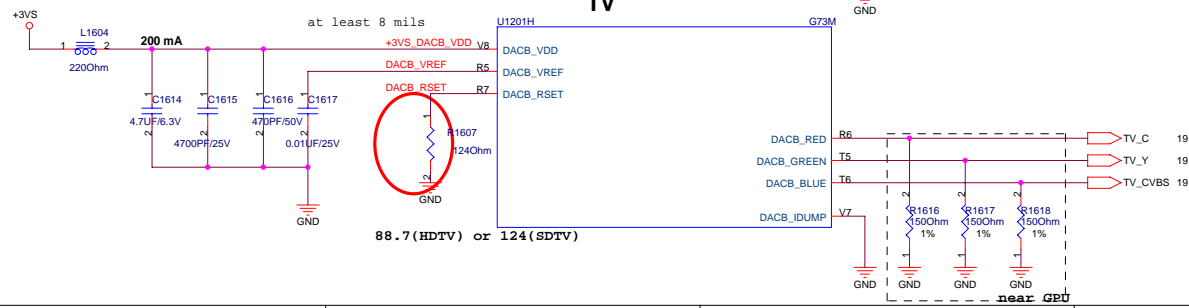
Add BackDrive

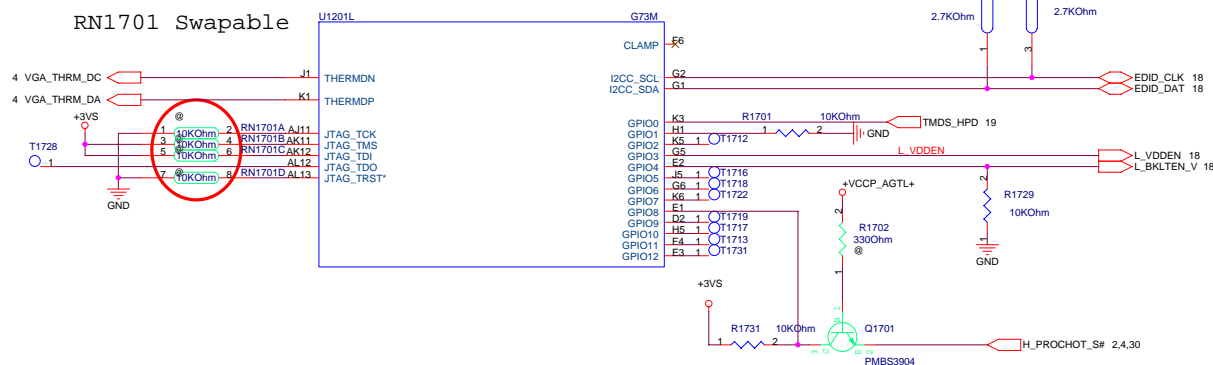
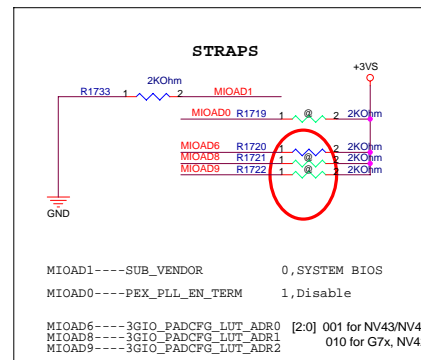
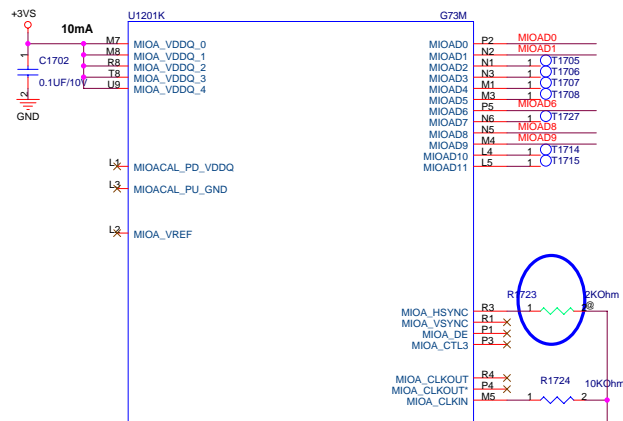
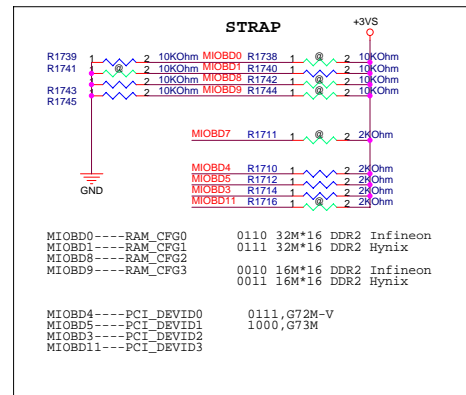
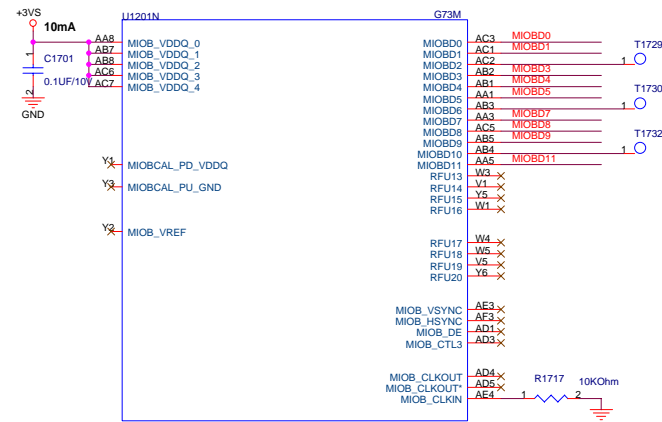


VGA



TV





GPIO0, 1 -- Hot Plug Detect (For DVI)
 GPIO2 -- Panel backlight brightness (PWM),
 GPIO3 -- Panel power enable
 GPIO4 -- Panel backlight ON/OFF
 GPIO5 -- GPU VID0
 GPIO6 -- GPU VID1
 GPIO7 -- GPU VID2 or MEM VID
 GPIO8 -- Thermal diode ALERT
 GPIO9 -- Fan control
 GPIO11 -- HDTV enable

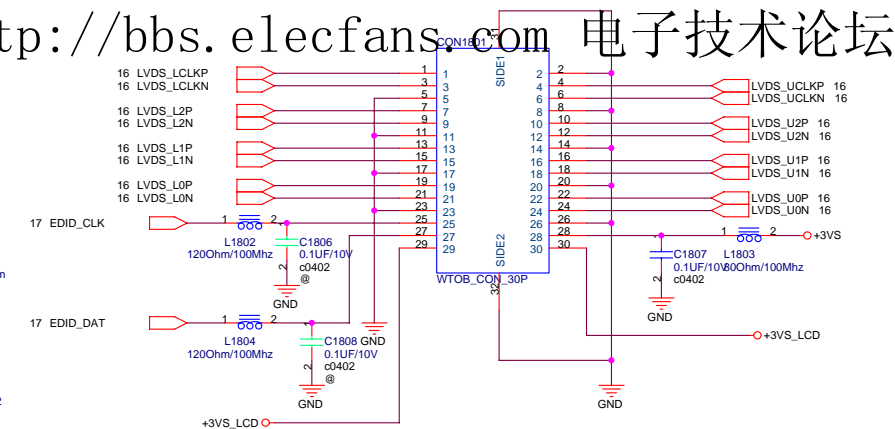
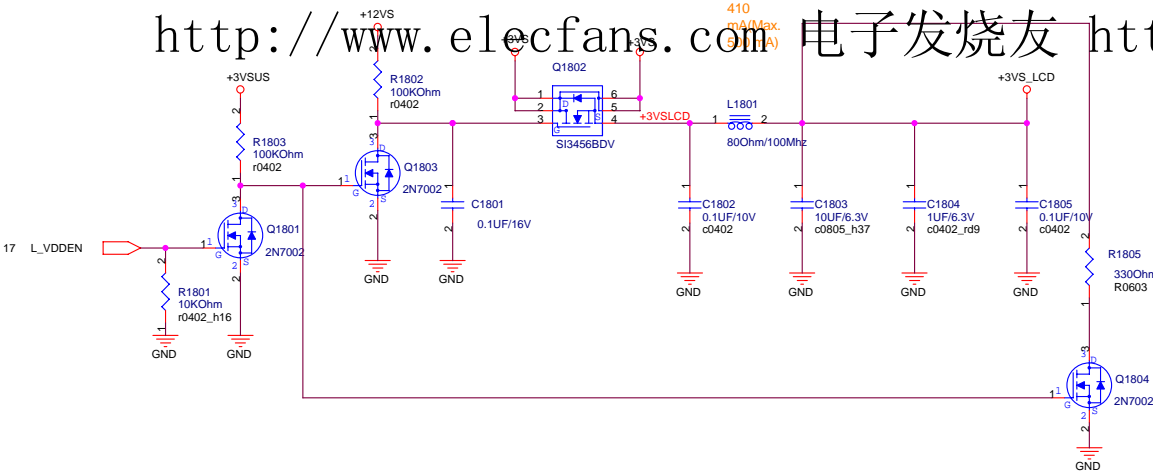
Internal Pull-down
 GPIO0, 1, 2, 4, 5, 6, 7

LCD Power

<http://www.elecfans.com> 电子发烧友

LCD LVDS Interface

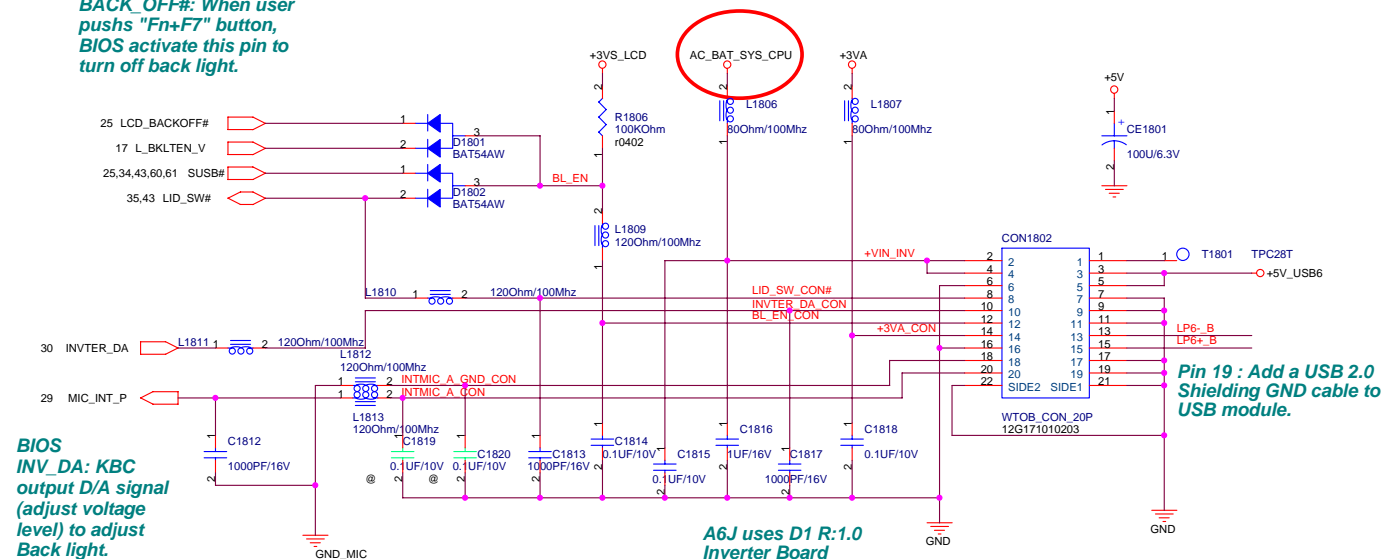
<http://bbs.elecfans.com> 电子技术论坛



Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

INVERTER Interface

BIOS BACK_OFF#: When user pushes "Fn+F7" button, BIOS activate this pin to turn off back light.



BIOS INV_DA: KBC output D/A signal (adjust voltage level) to adjust Back light.

For EMI

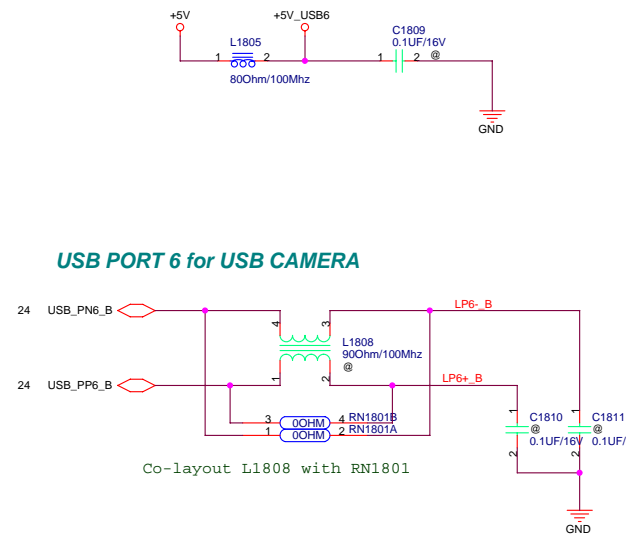


A6J uses D1 R:1.0 Inverter Board

Pin 19 : Add a USB 2.0 Shielding GND cable to USB module.

A6J doesn't support USB WLAN function!

USB PORT 6 for USB CAMERA



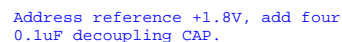
Co-layout L1808 with RN1801

<Variant Name>

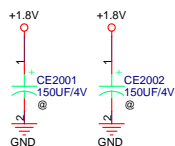
ASUS		Title : LVDS & INVERTER	
<OrgName>		Engineer: Charles Lee	
Size	Project Name	Rev	
Custom	A6Jc	2.1	
Date: Thursday, January 19, 2006	Sheet	18	of 63



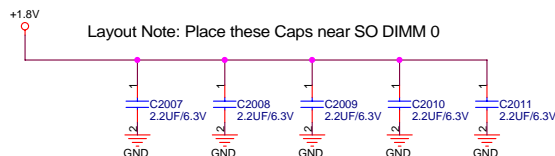
电子技术论坛



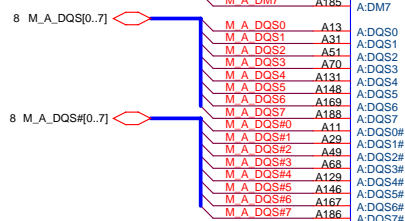
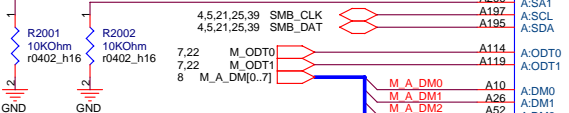
8,22	M_A_BS#2	A16	A15
8,22	M_A_BS#0	A107	A_BA0
8,22	M_A_BS#1	A106	A_BA1
7,22	M_CS#0	A110	A_S0#
7,22	M_CS#1	A115	A_S1#
7	M_CLK_DDR0	A30	CKD0
7	M_CLK_DDR#0	A32	CKD#0
7	M_CLK_DDR1	A164	CK1
7	M_CLK_DDR#1	A166	CK#1
7,22	M_CKE0	A79	CKE0
7,22	M_CKE1	A80	CKE1
8,22	M_A_RAS#	A113	A_CAS#
8,22	M_A_RAS#	A108	A_RAS#
8,22	M_A_WE#	A109	A_WE#



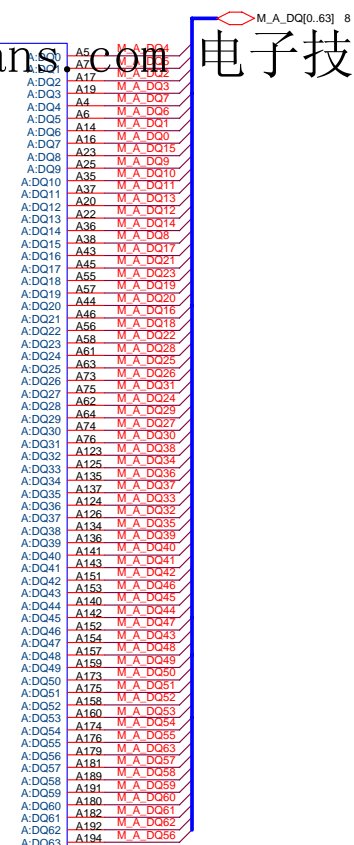
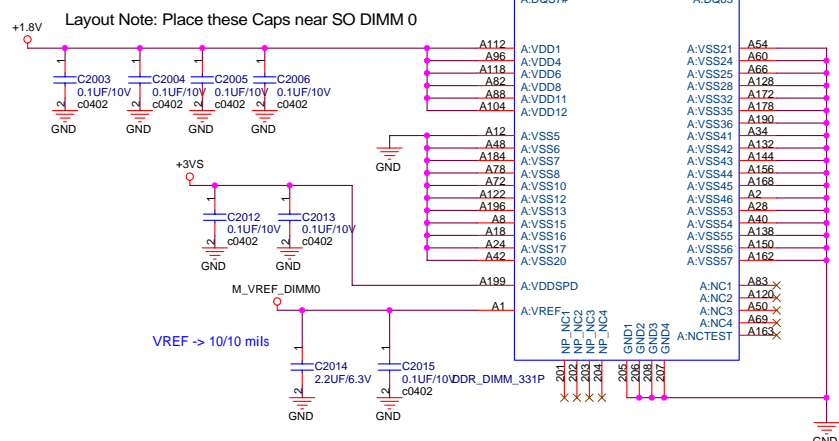
Layout Note: Place these Caps near SO DIMM 0



SO-DIMM 0 is placed farther from the GMCH than SO-DIMM 1



Layout Note: Place these Caps near SO DIMM 0



<Variant Name>



Title : DDR2 SO-DIMM_0

Engineer: *Charles Lee*

Size	5
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Size	Project Name
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Custom

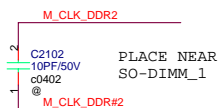
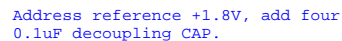
Date: Thursday, January 19, 2006

Rev
2.1Rev
2.1

Date: Thursday, January 19, 2006 Sheet 20 of 63

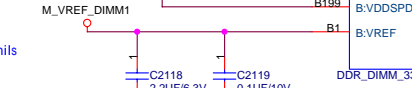
63

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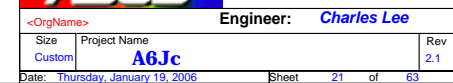


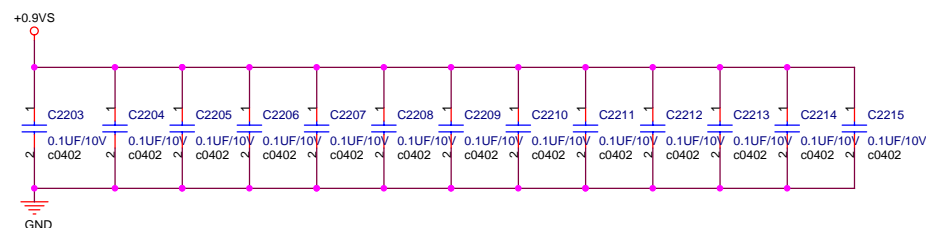
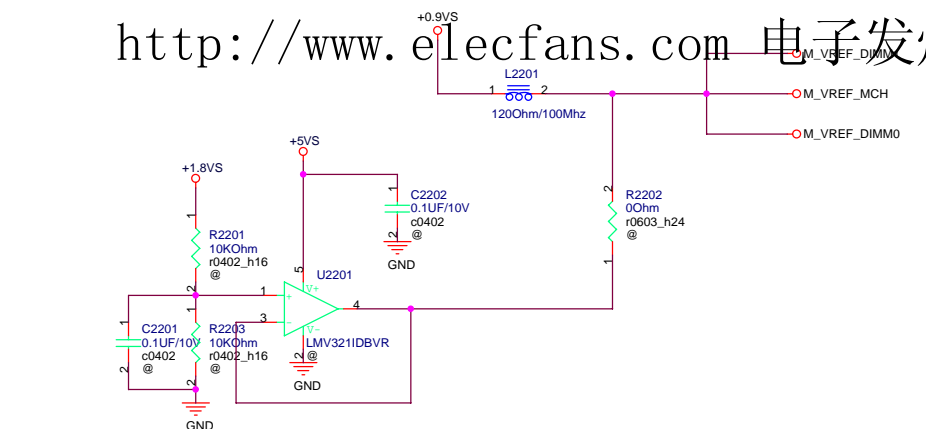
The diagram shows a +1.8V supply connected to a horizontal bus. Four decoupling capacitors, labeled C2103, C2104, C2105, and C2106, are connected in parallel between this bus and ground (GND). Each capacitor is specified as 0.1UF/10V and c0402.

The diagram shows a +1.8V power plane with five decoupling capacitors (C2113, C2114, C2115, C2116, C2117) connected to ground. Each capacitor is labeled with its value: 2.2UF/6.3V.

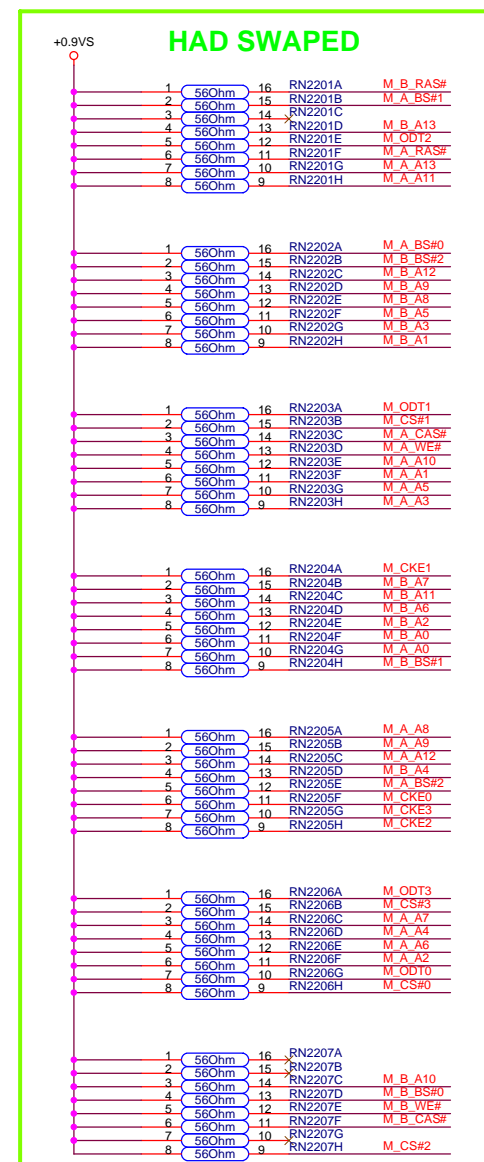
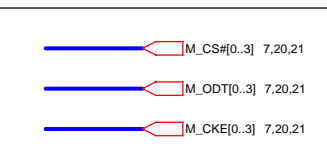
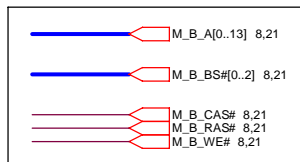
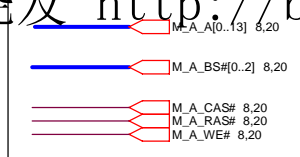
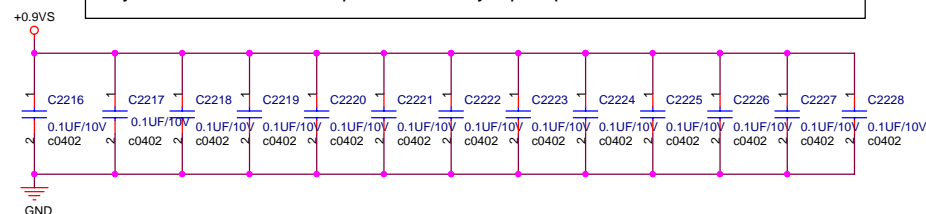


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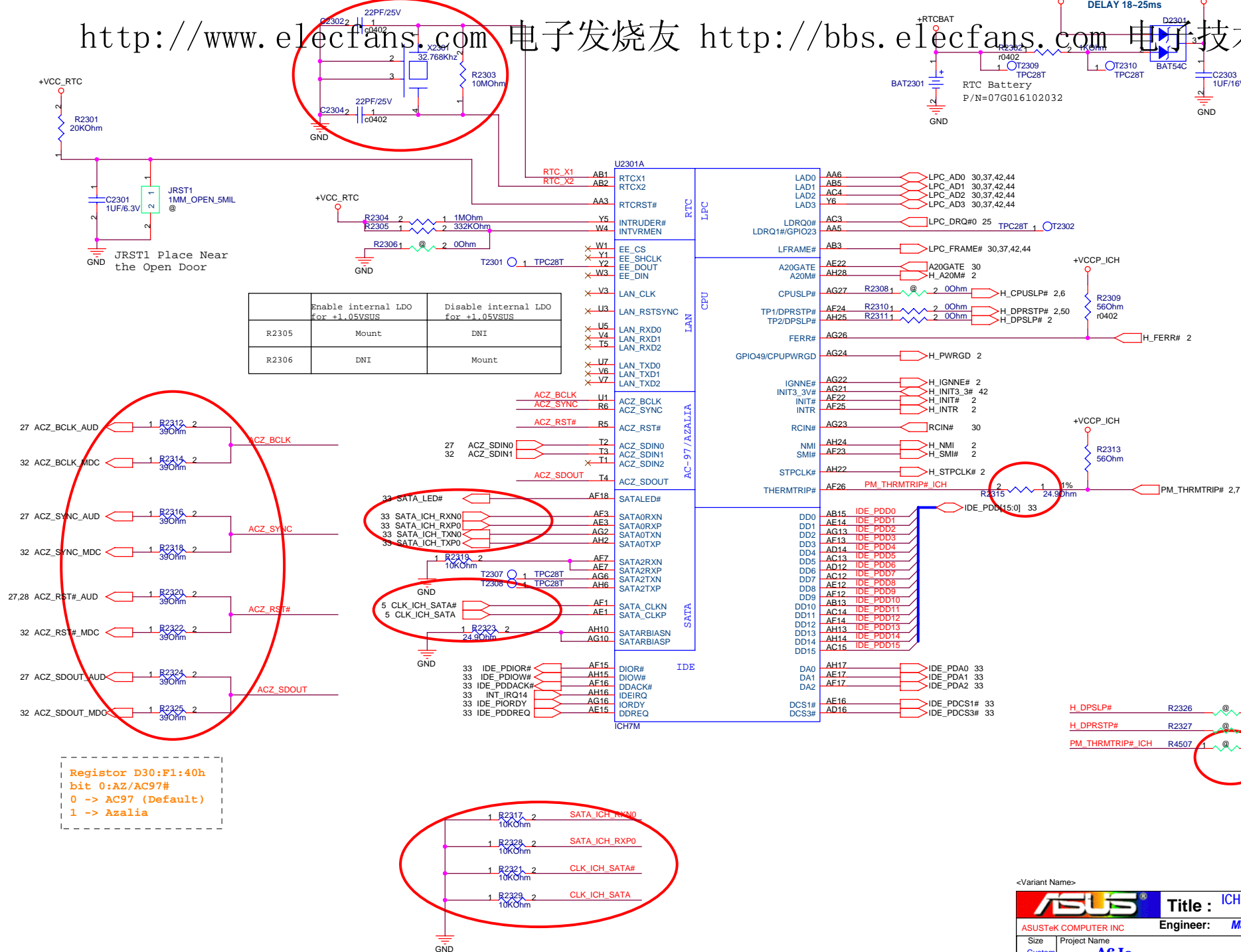


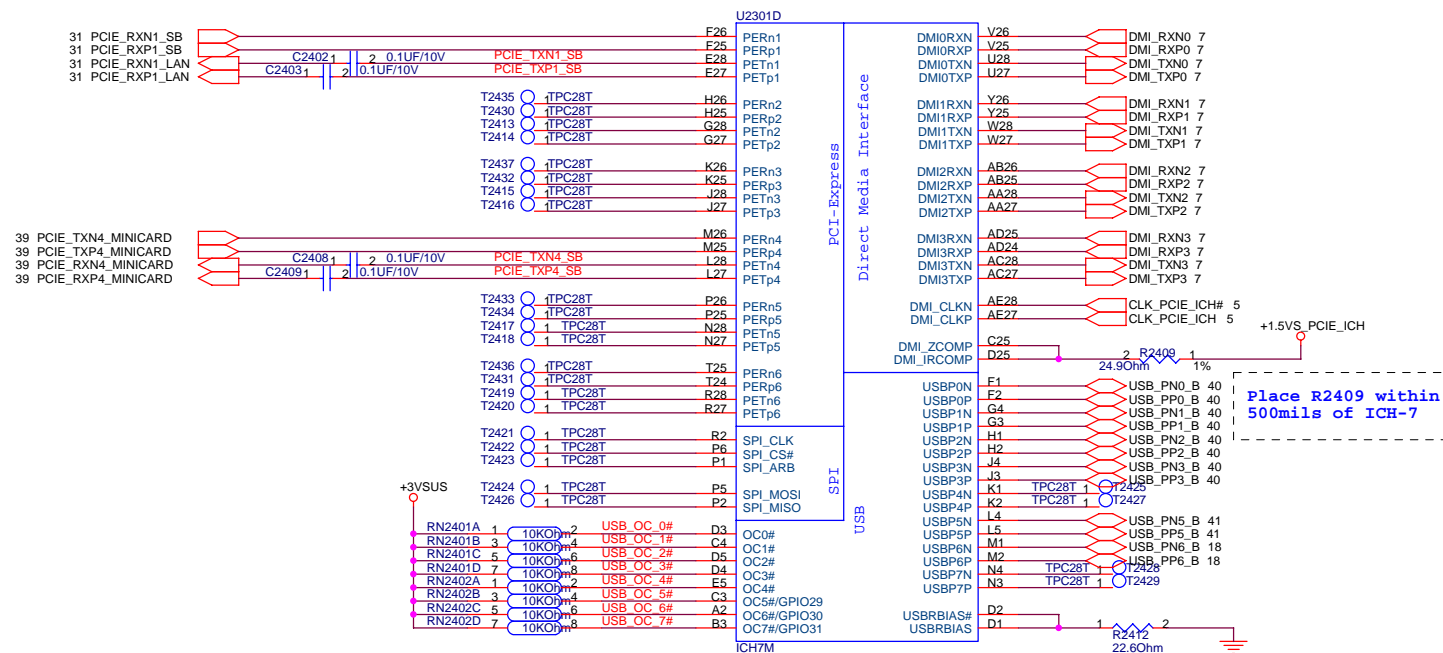
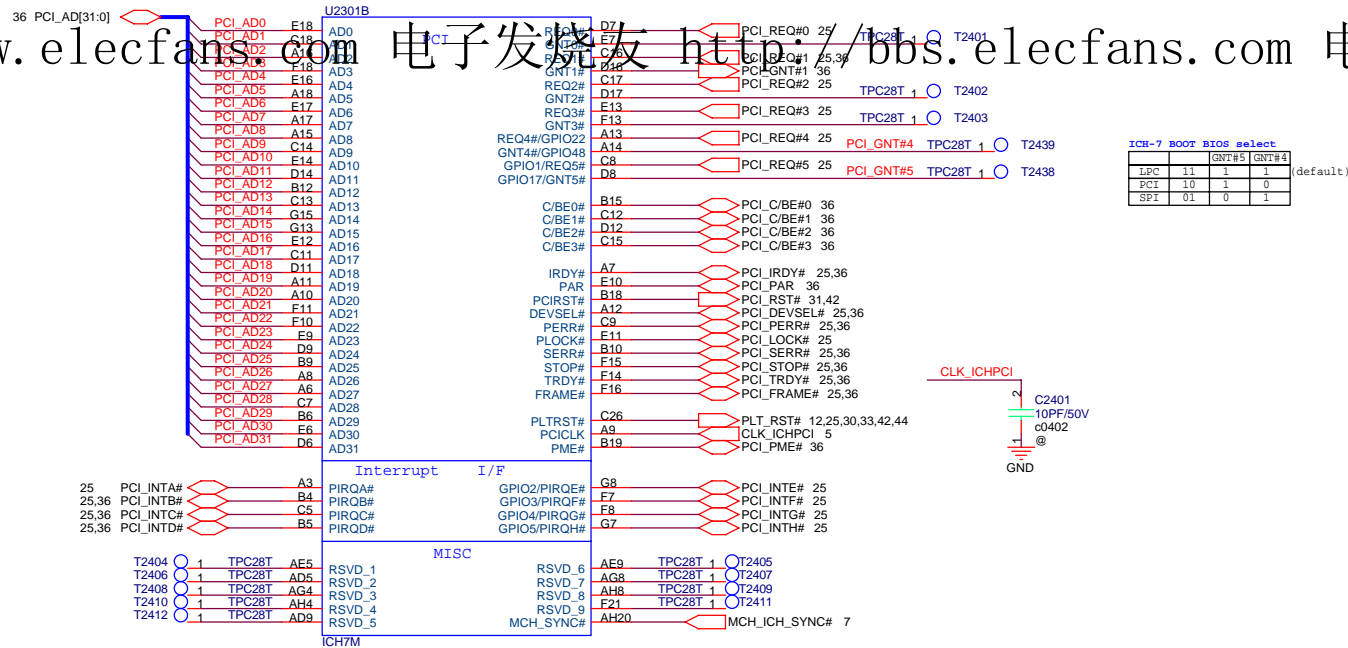
Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS



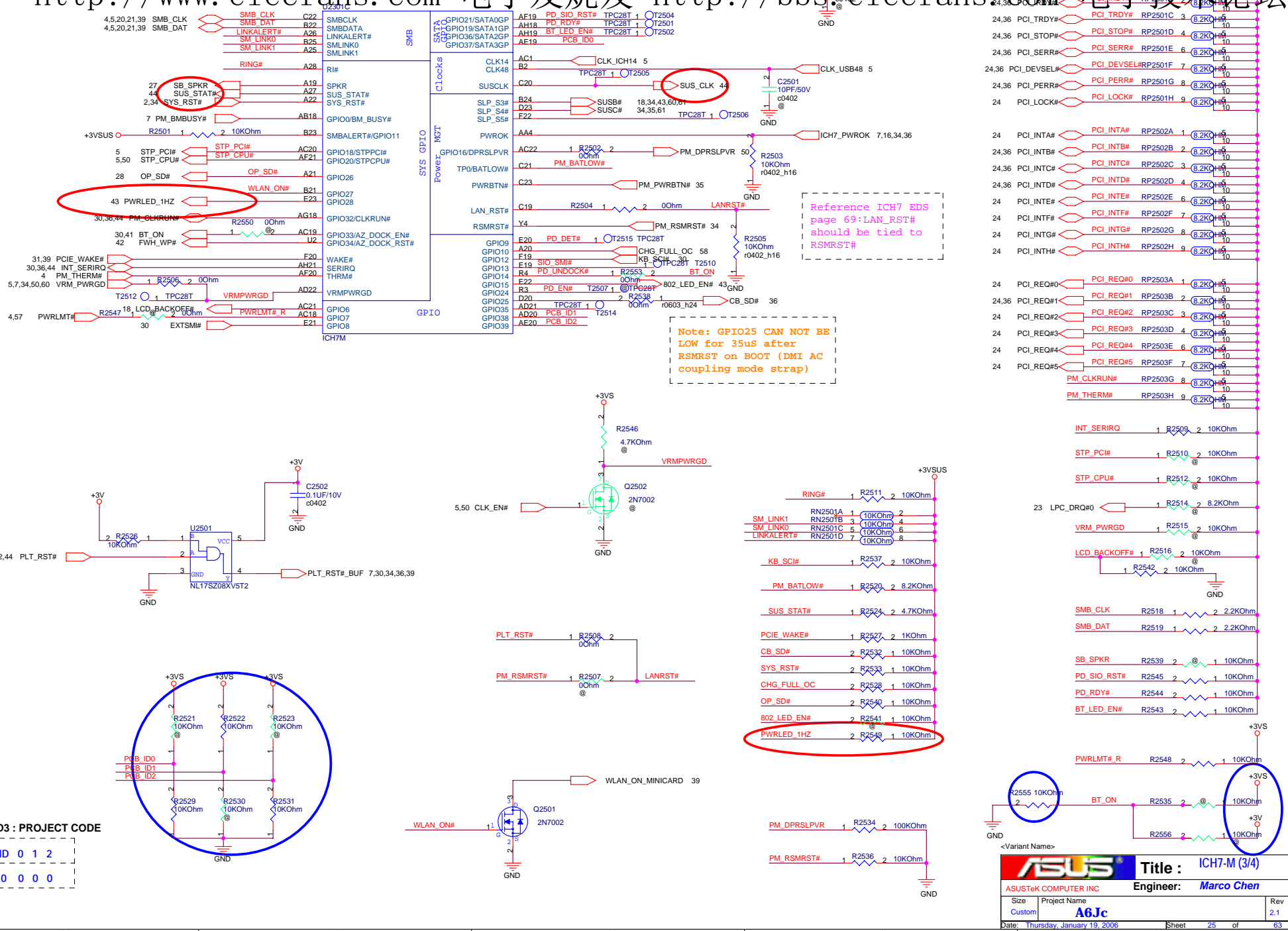
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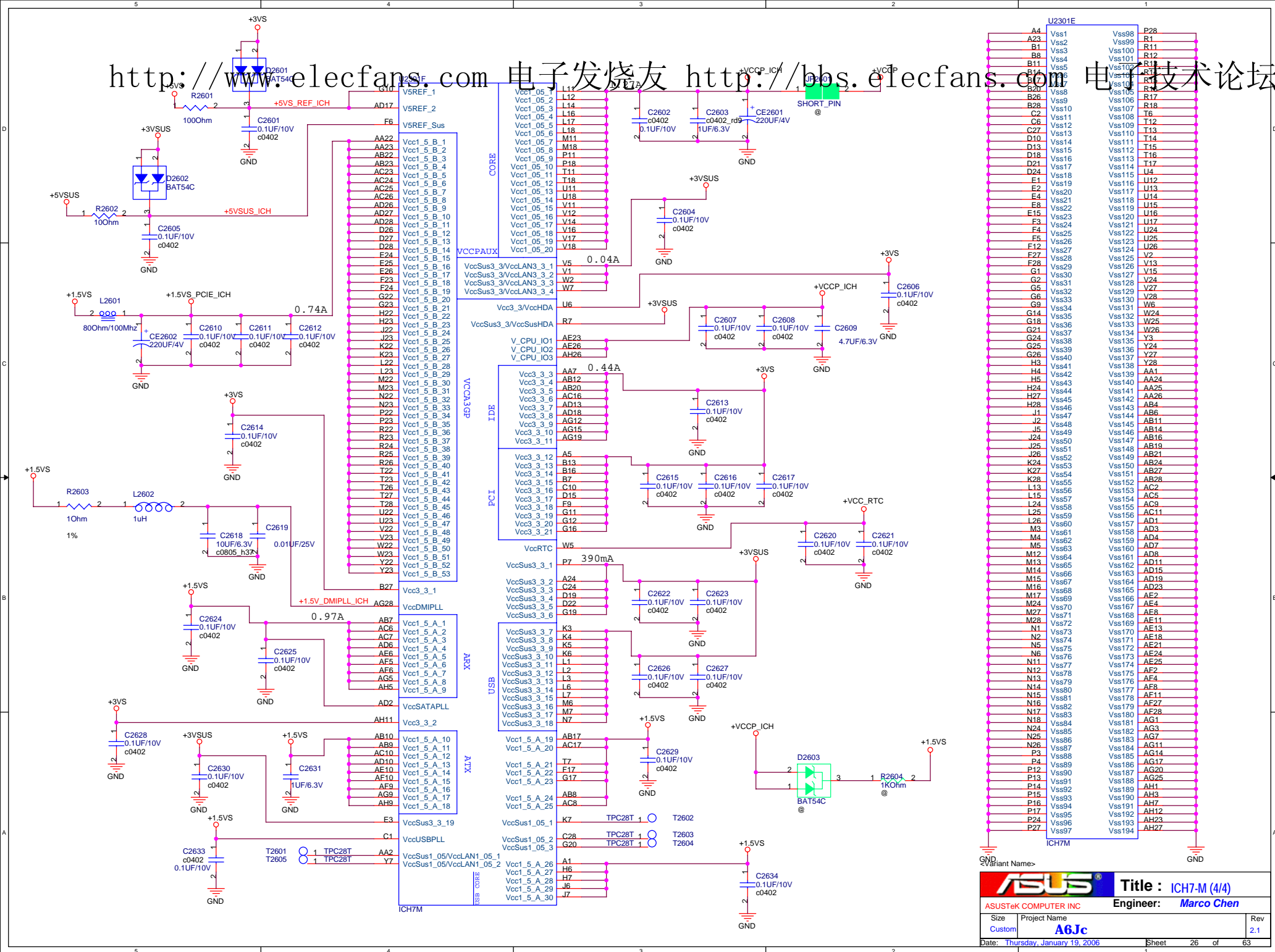




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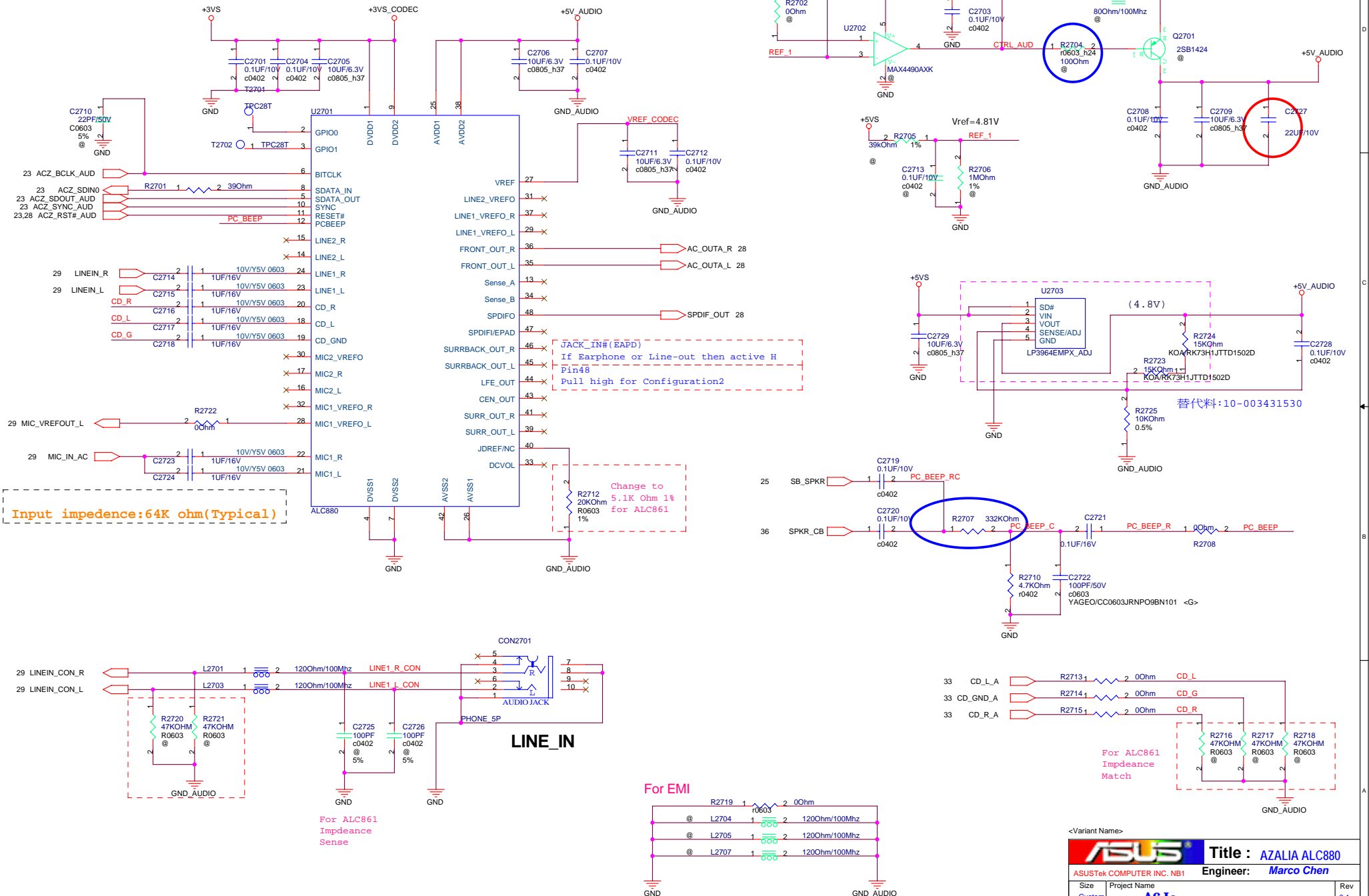


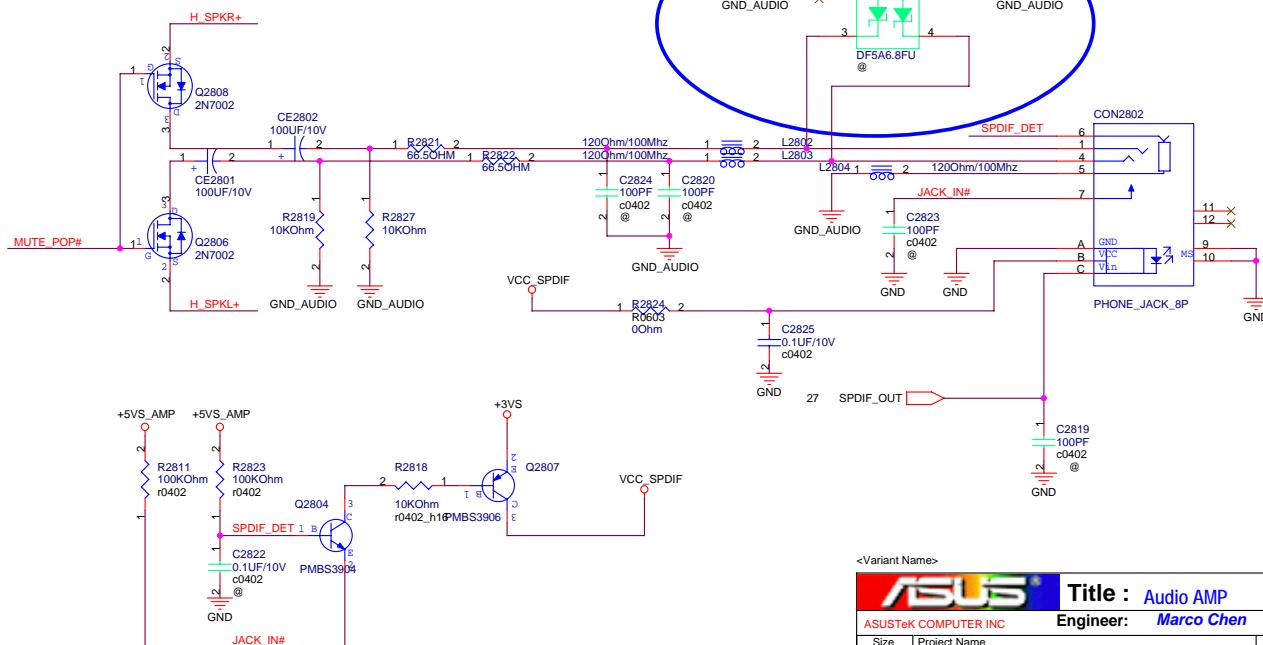
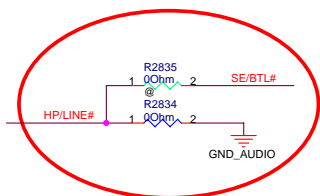
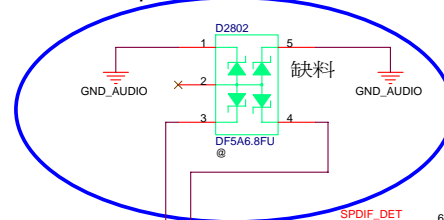
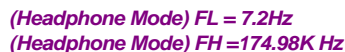
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Place U2802near U2801

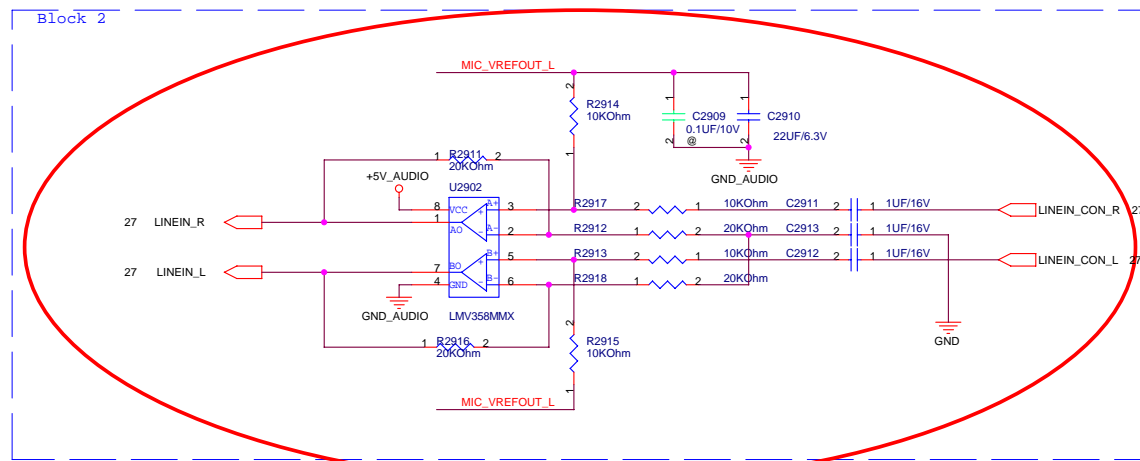
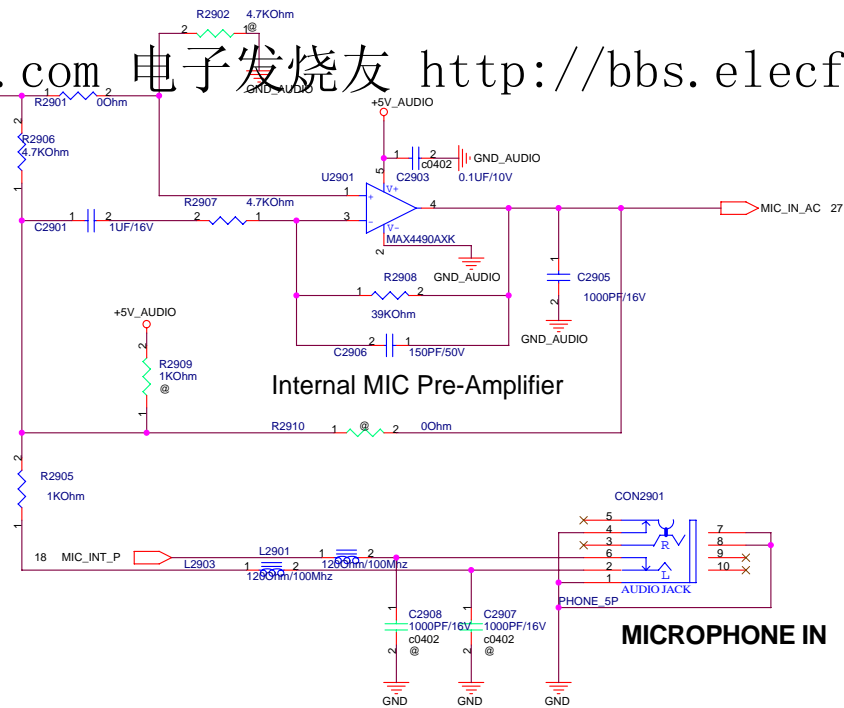
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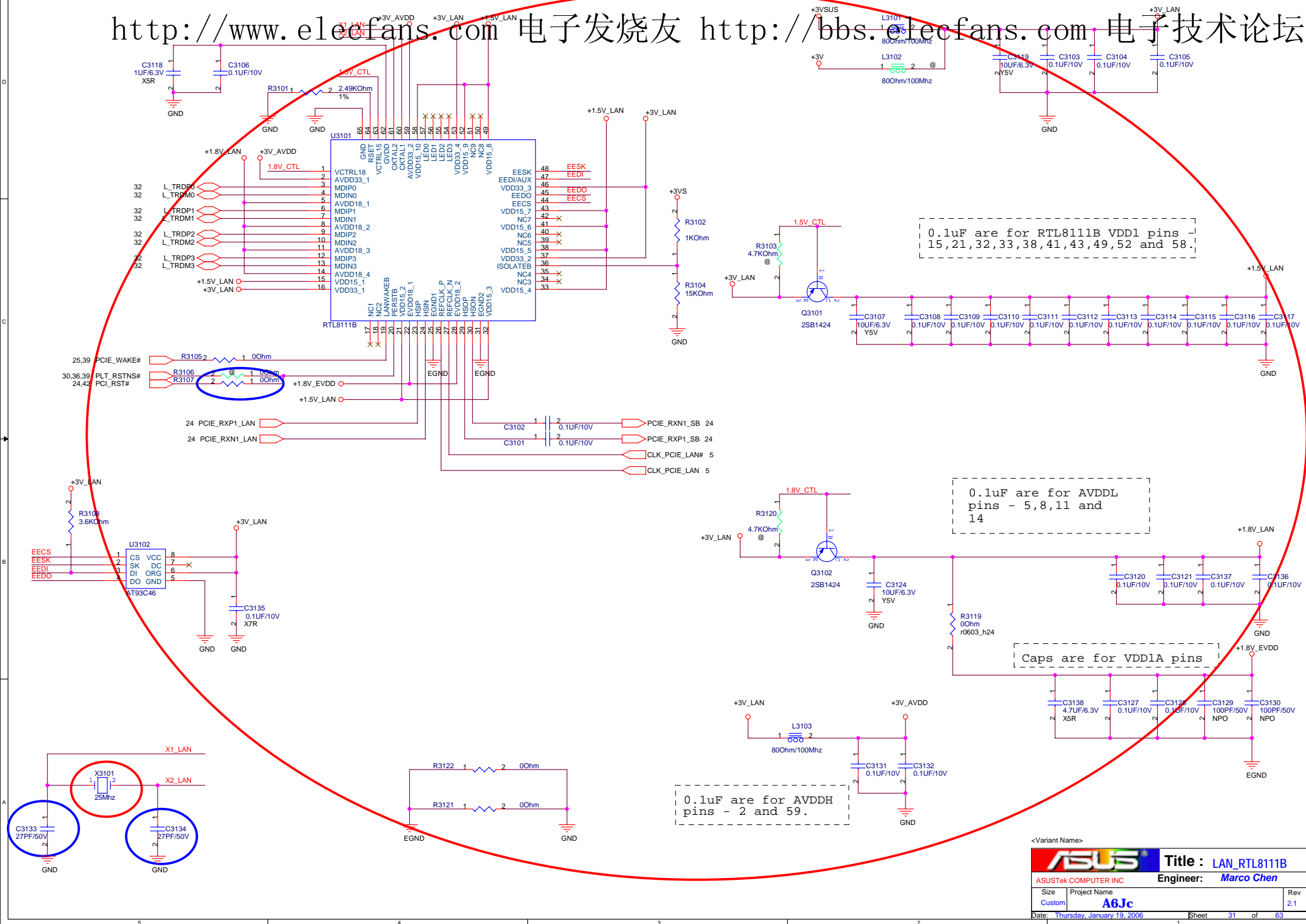
	SE/BTL#	SPDIF_IN
SPDIF Mode	H	Hi-Z
HP Mode	H	L
SPK Mode	L	X

(Microphone)FL = 33.86 Hz
(Microphone)FH = 27.2K Hz



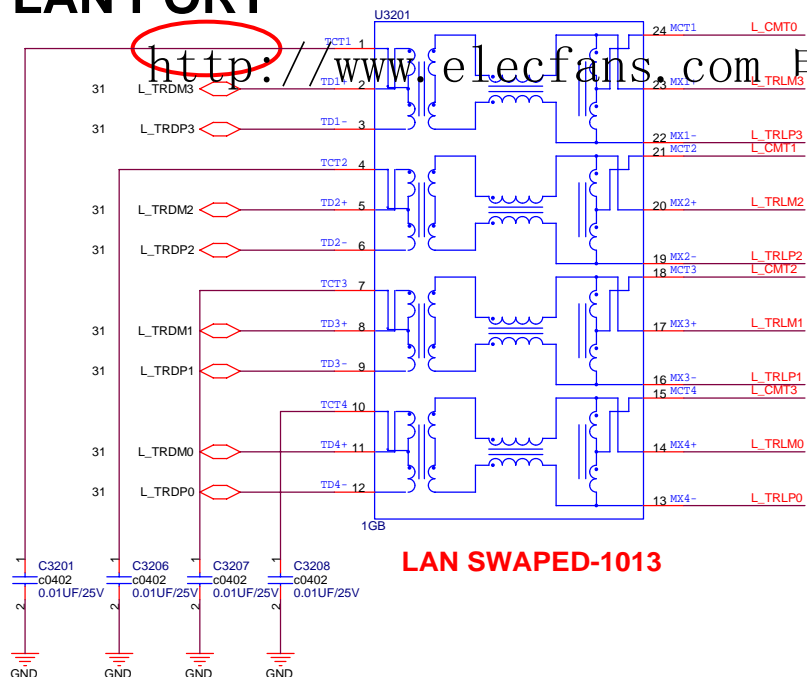
<Variant Name>

ASUS		Title : MICROPHONE	
ASUSTek COMPUTER INC		Engineer: Marco Chen	
Size Custom	Project Name A6Jc	Rev 2.1	
Date: Thursday, January 19, 2006		Sheet 29 of 63	

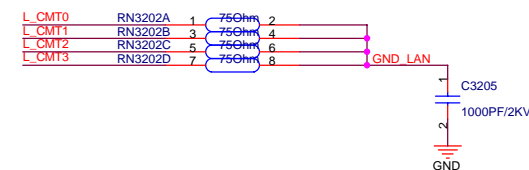
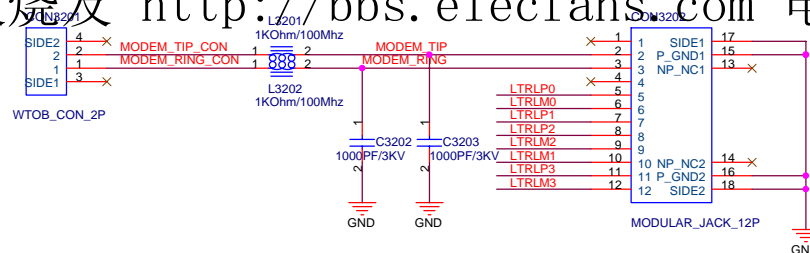


LAN PORT

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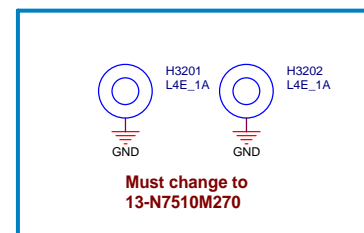
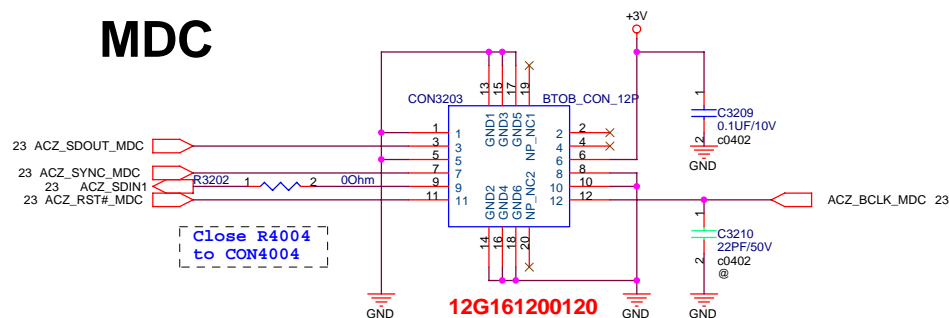
LAN SWAPED-1013



FOR EMI

L_TRLM2	1	0	2	RN3201A	LTRLM2
L_TRLP2	3	0	4	RN3201B	LTRLP2
L_TRLP0	5	0	6	RN3201C	LTRLP0
L_TRLP1	7	0	8	RN3201D	LTRLP1
L_TRLM1	1	0	3	RN3203A	LTRLM1
L_TRLM3	3	0	4	RN3203B	LTRLM3
L_TRLP3	5	0	6	RN3203C	LTRLP3
	7	0	8	RN3203D	

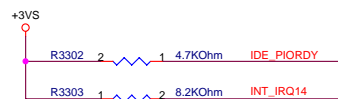
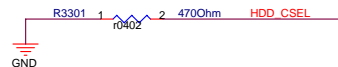
MDC



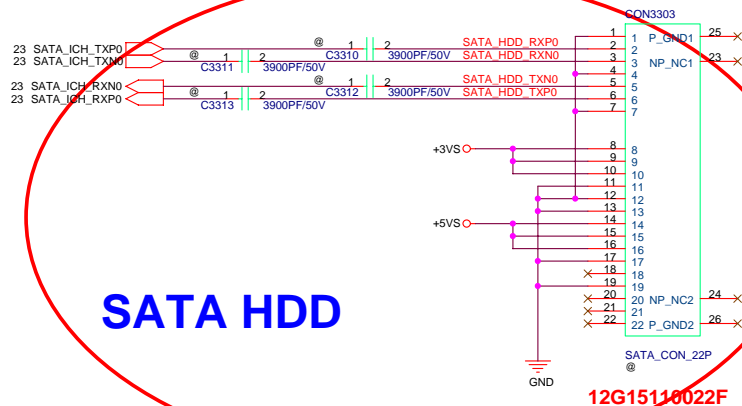
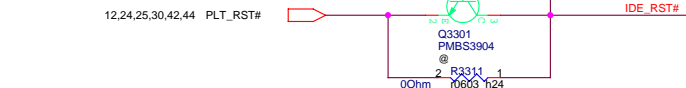
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HDD_CSEL : Pull-Down HDD as Master



12,24,25,30,42,44 PLT_RST#



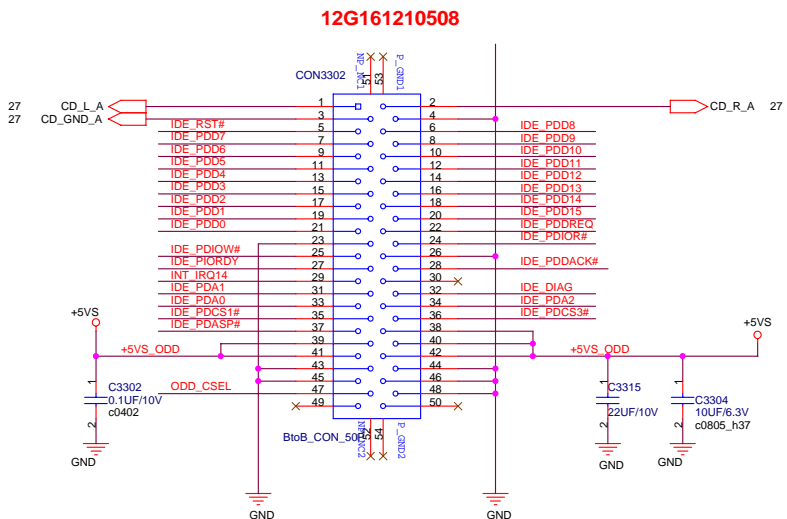
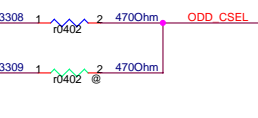
SATA HDD

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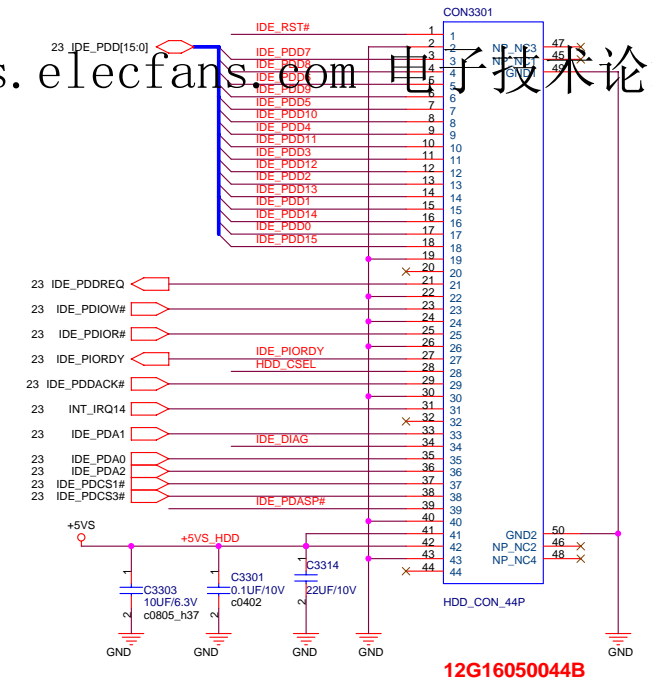
PATA HDD

CD-ROM

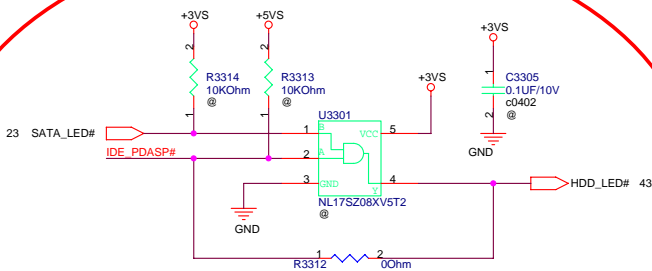
ODD_CSEL : Pull-Up, CDROM as Slave, Pull-Down, CDROM as Master



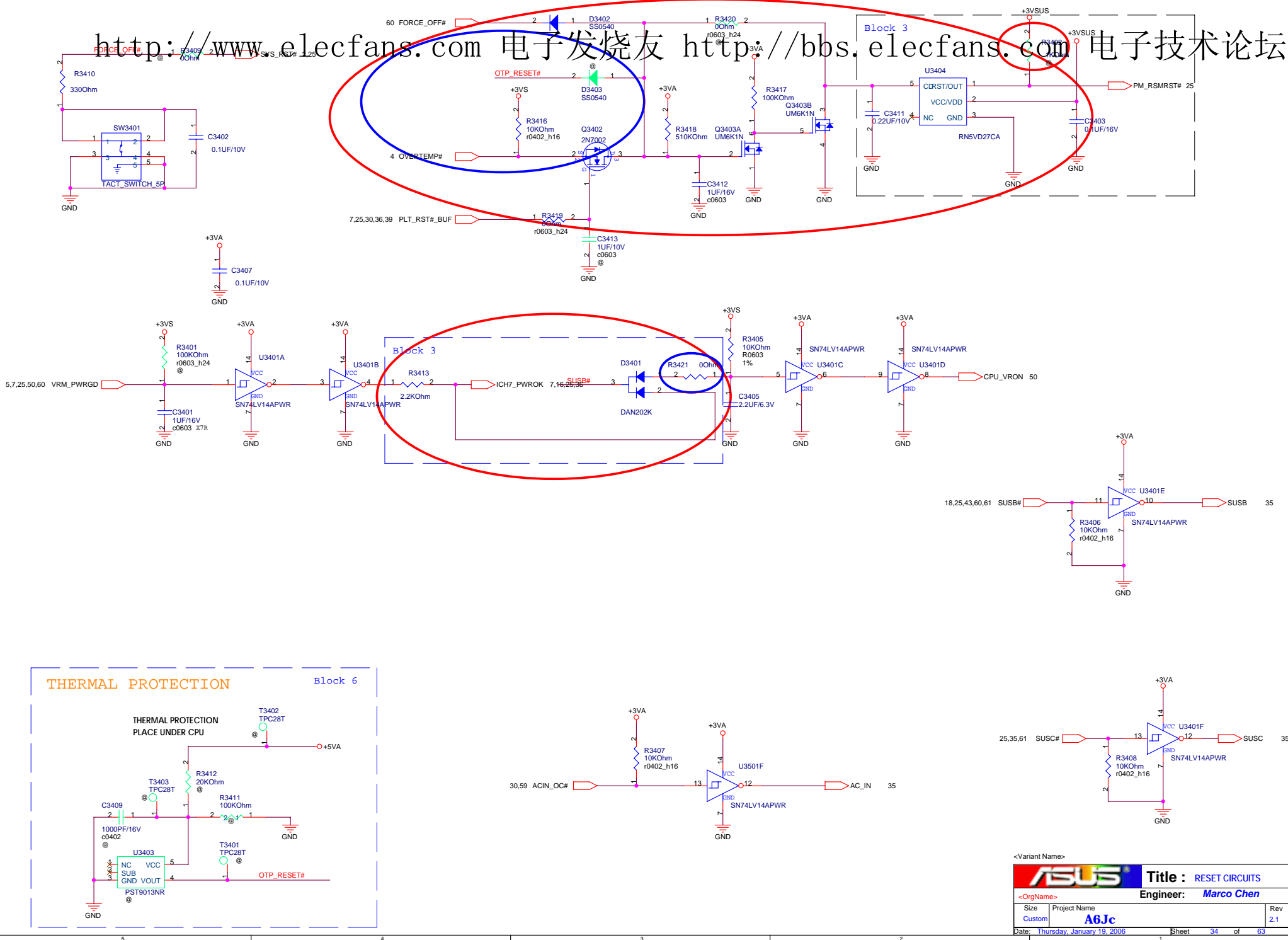
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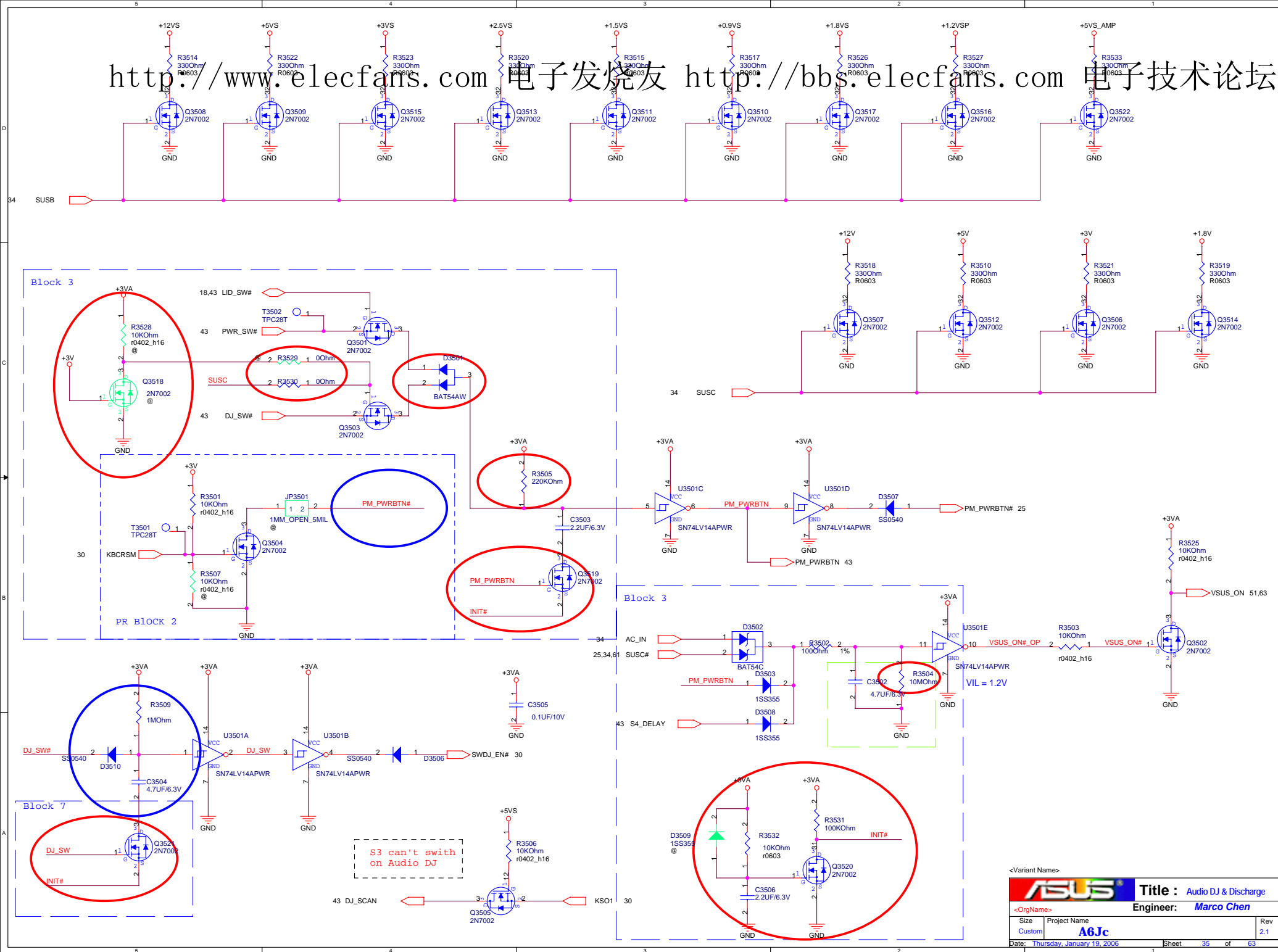
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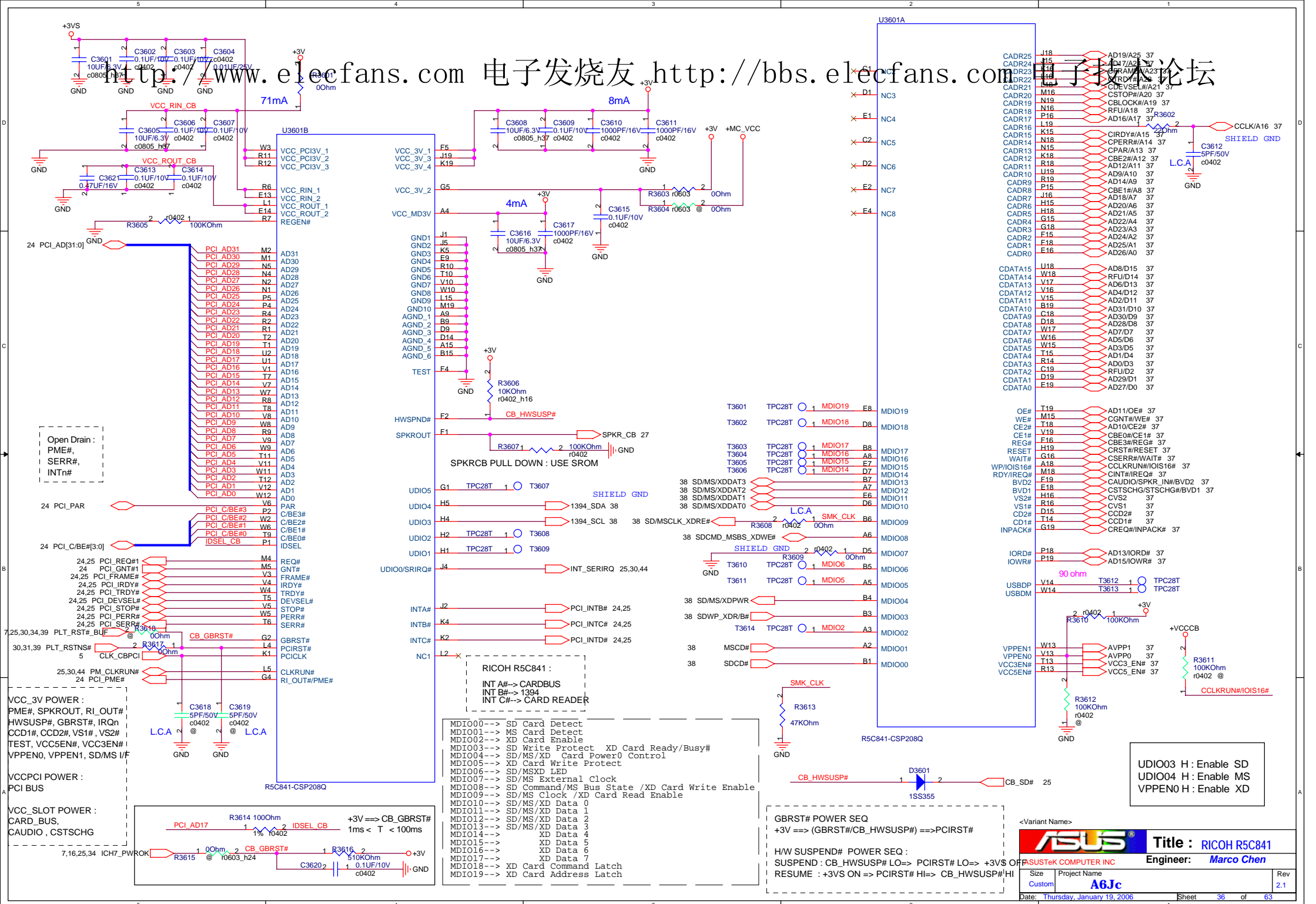


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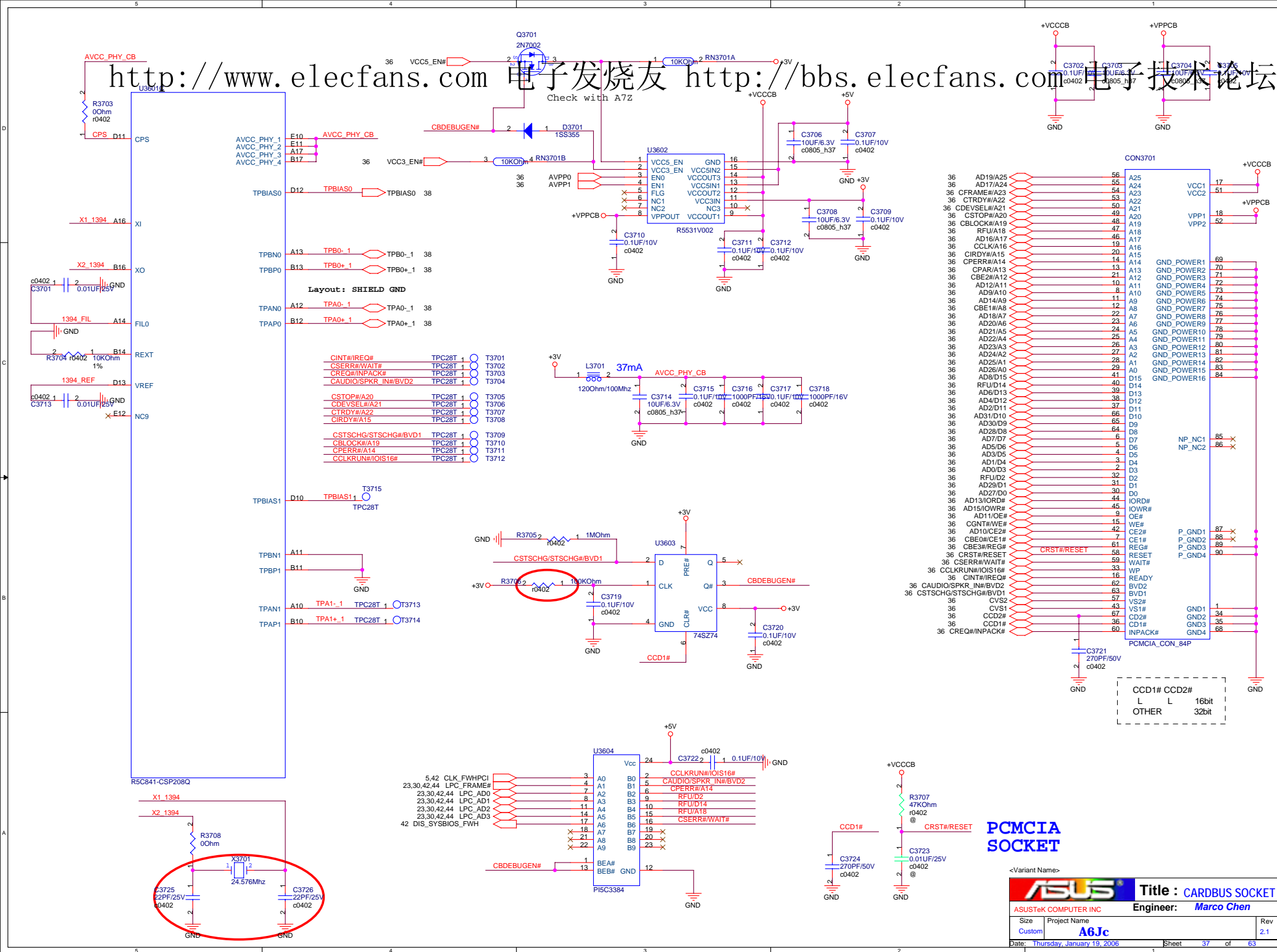


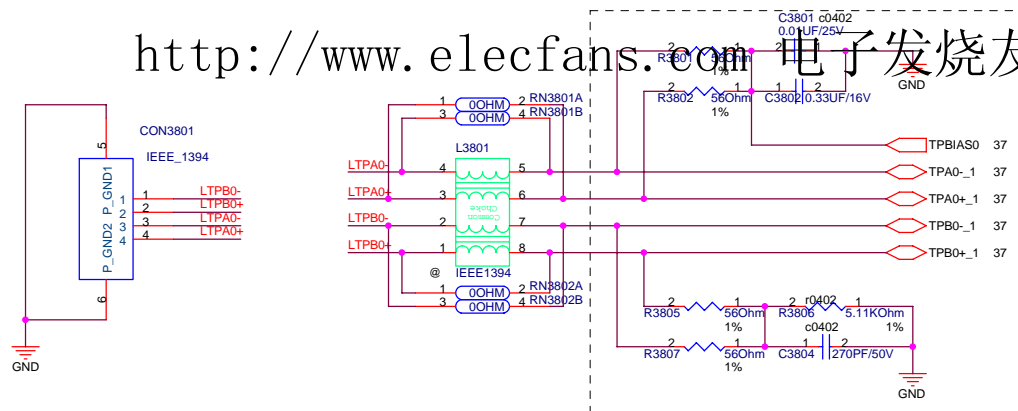
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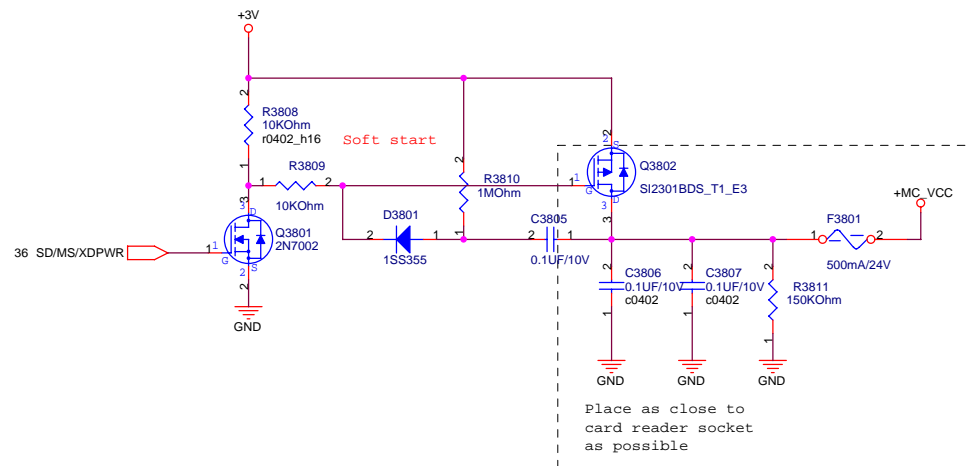
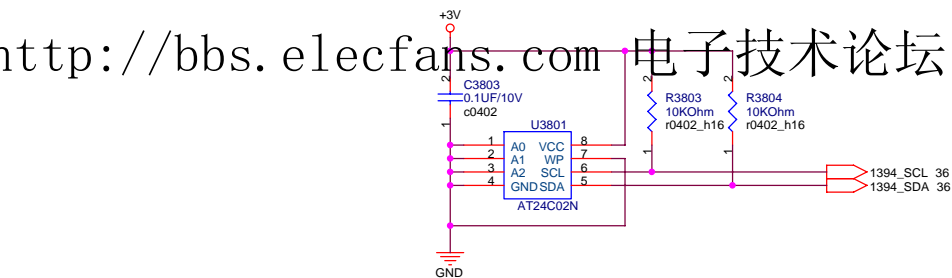
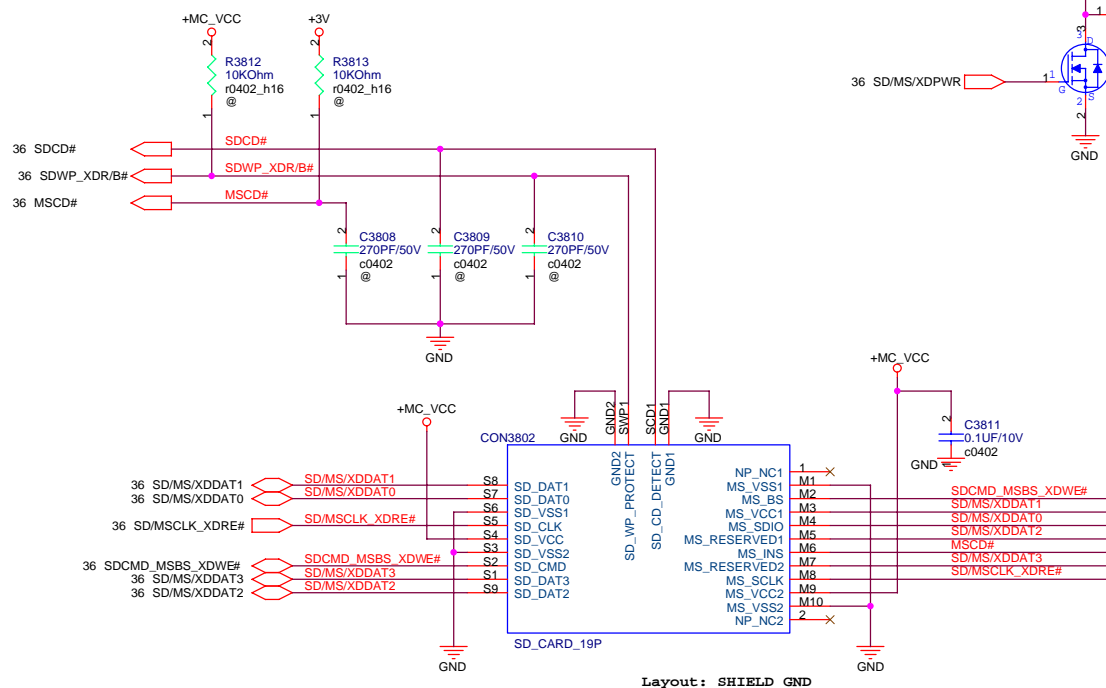


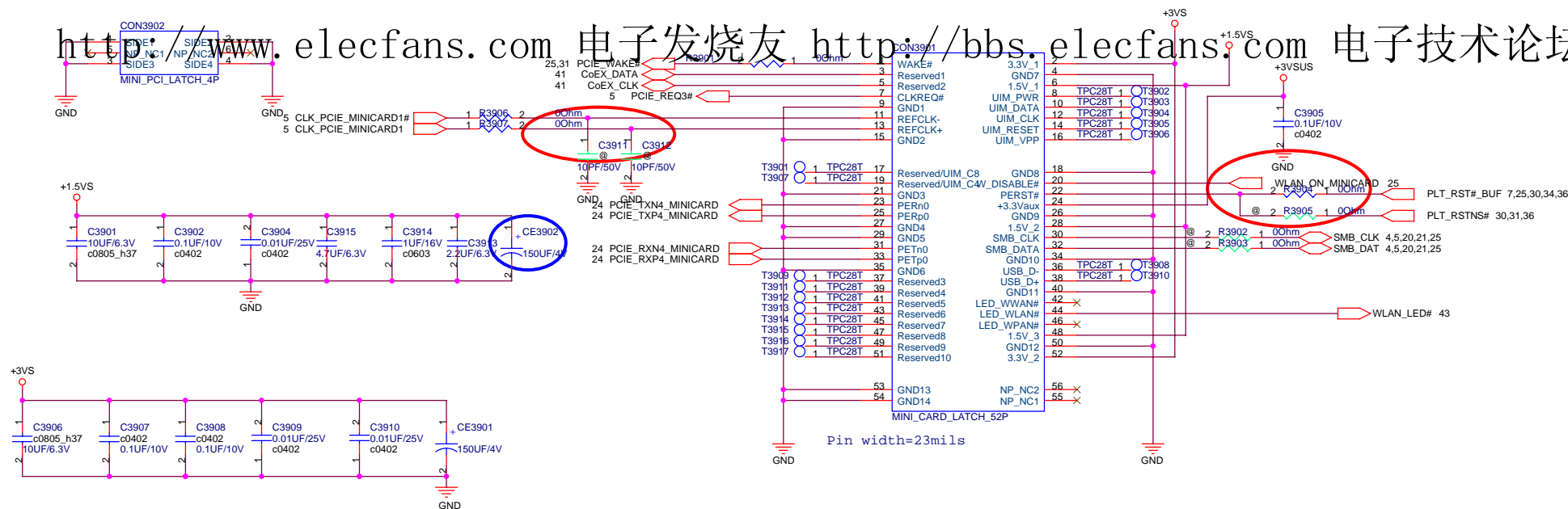
http://www.elecfans.com 电子发烧友 http://bbs.elecfans.com 电子技术论坛





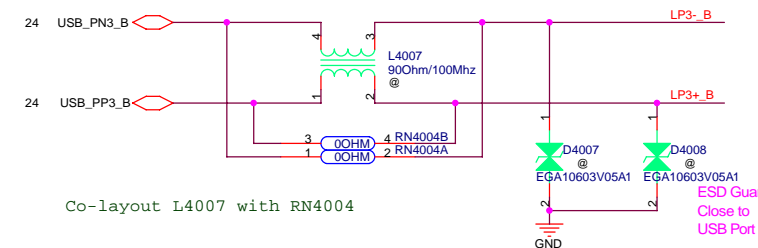
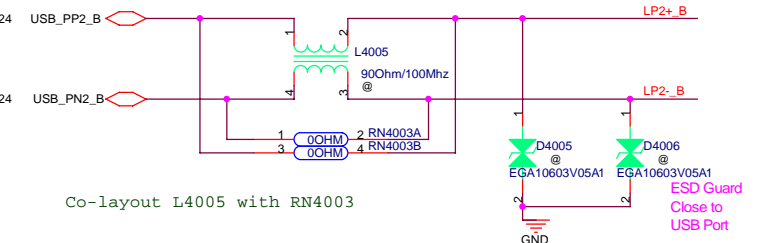
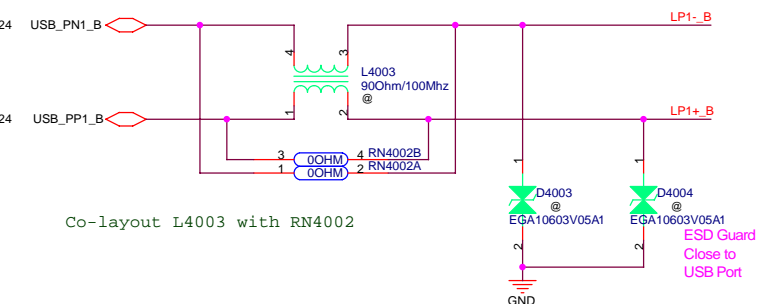
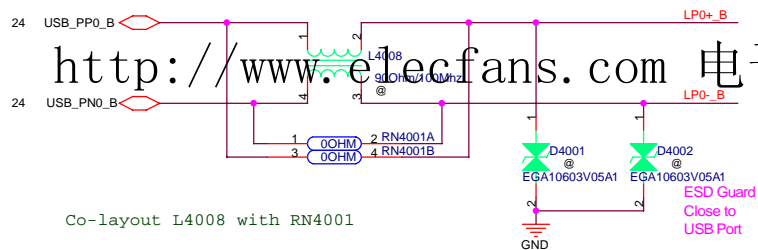
1. CLOSE TO R5C841
2. The area is as compact as possible, length < 10 mm
3. TPA Pair and TPB pair mismatch < 2.5mm
4. No via recommend , maxmium is one.
5. Total length < 50 mm
6. Differential impedance is 110+/- 6 ohm
7. TPA Pair trace or TPB pair trace mismatch < 1.25mm



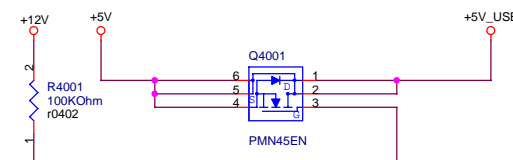
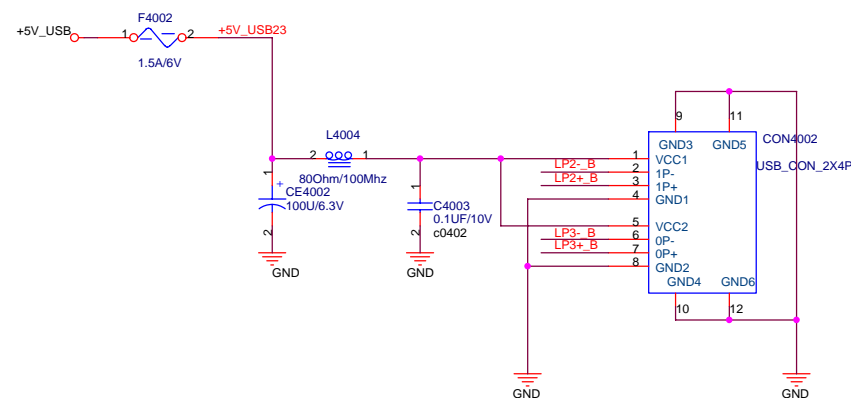
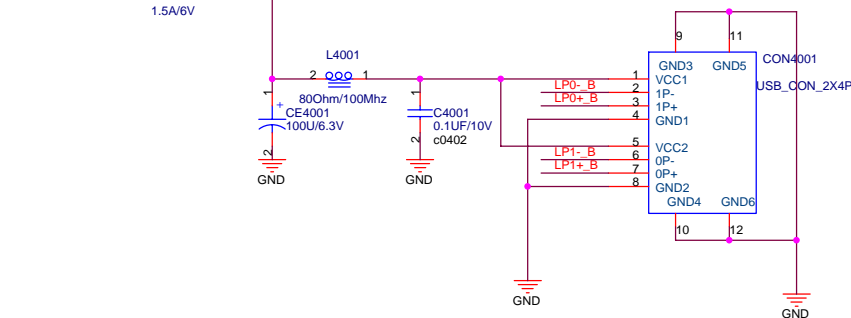


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ASUSTeK COMPUTER INC		Engineer: Marco Chen	
Size	Project Name	Rev	
Custom	A6Jc	2.1	
Date: Thursday, January 19, 2006	Sheet	39	of 63



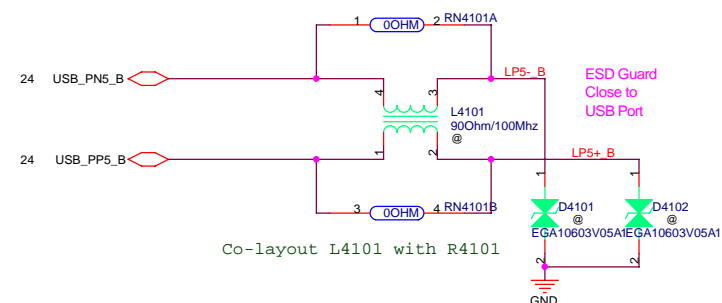
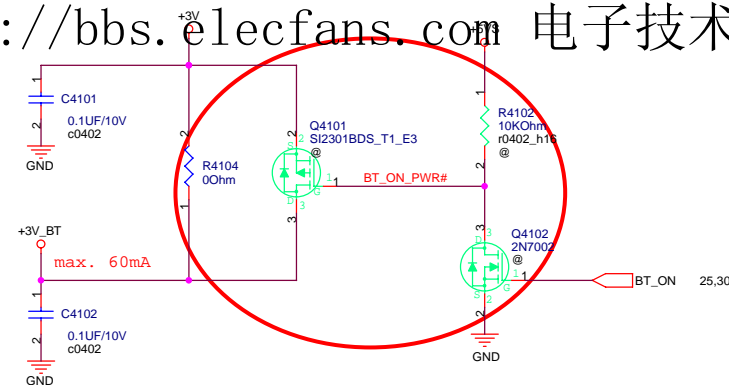
4P2R array resister
co-layout with common choke



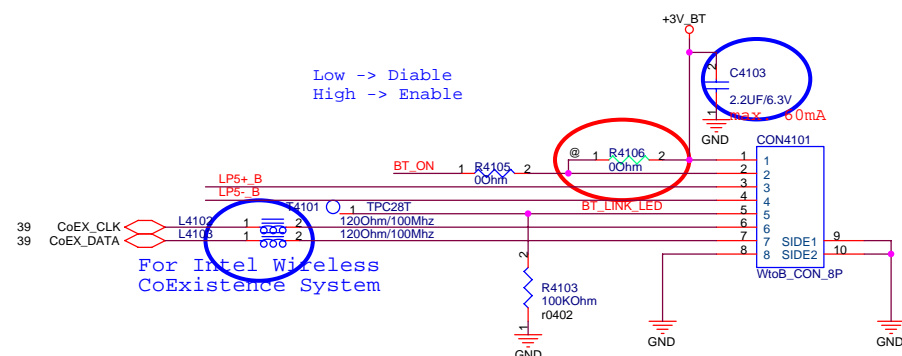
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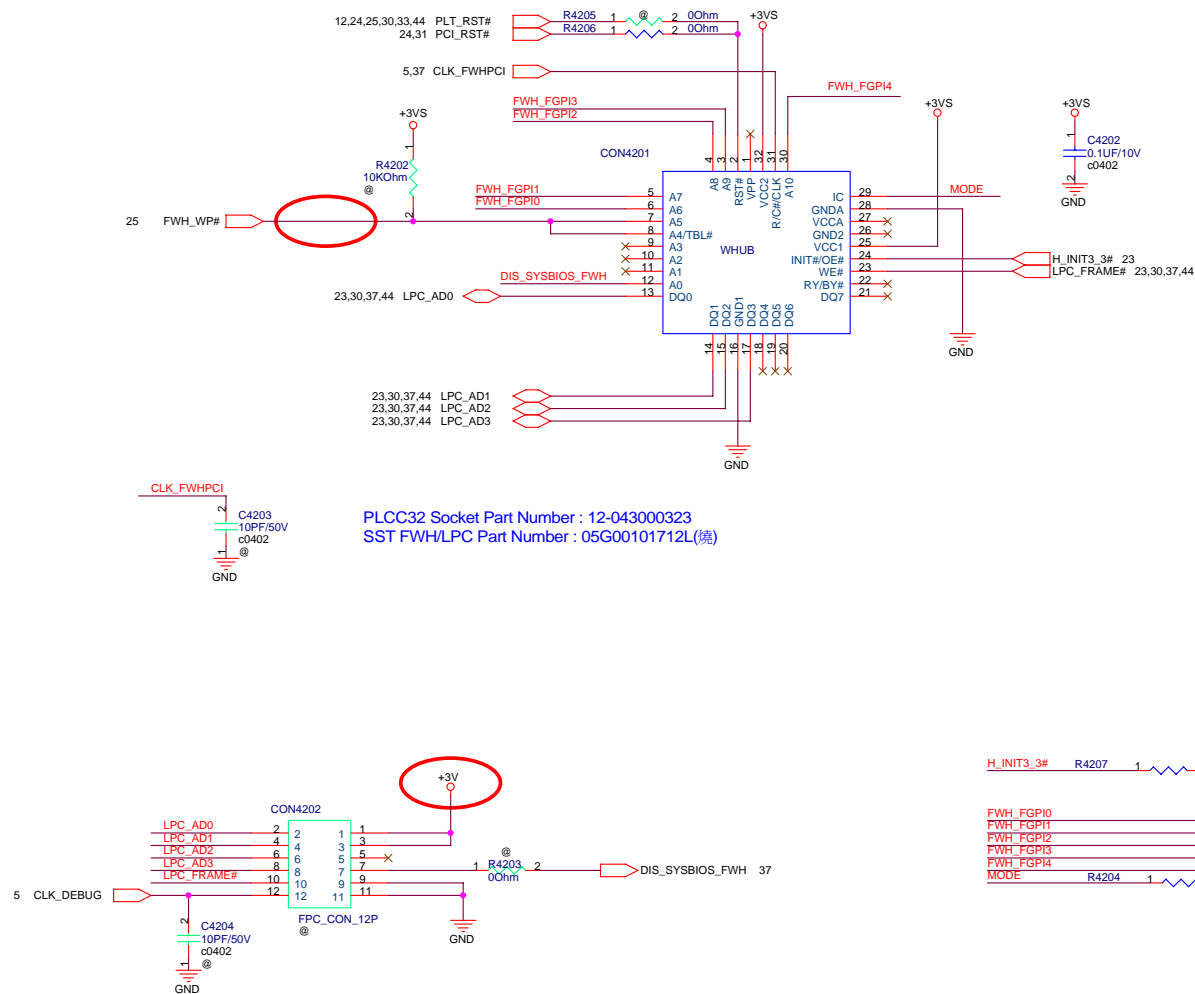
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ASUSTeK COMPUTER INC		Engineer: Marco Chen	
Size	Project Name	Rev	
Custom	A6Jc	2.1	
Date: Thursday, January 19, 2006	Sheet	40	of 63

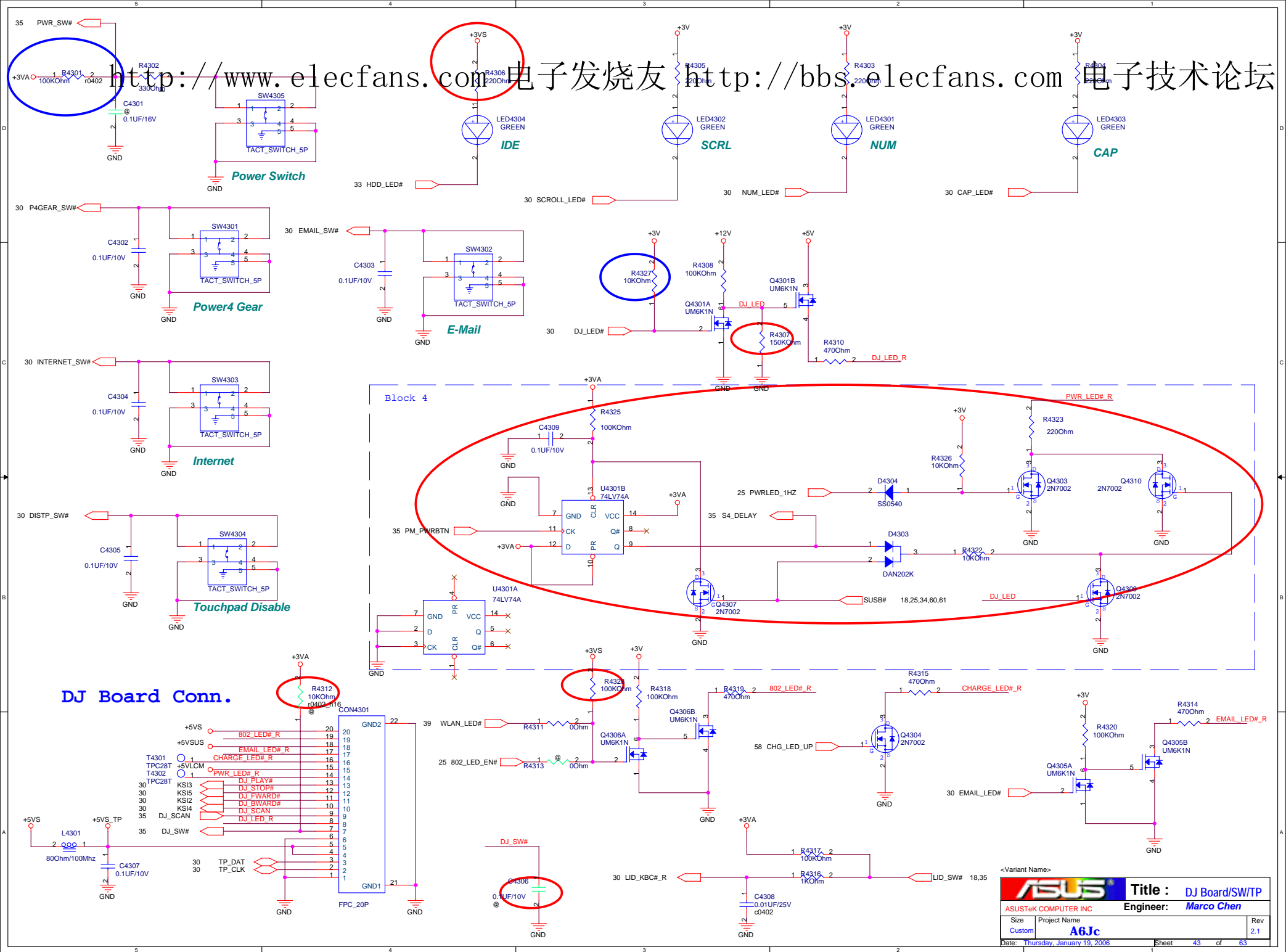
BT ON/OFF Control




Bluetooth Module



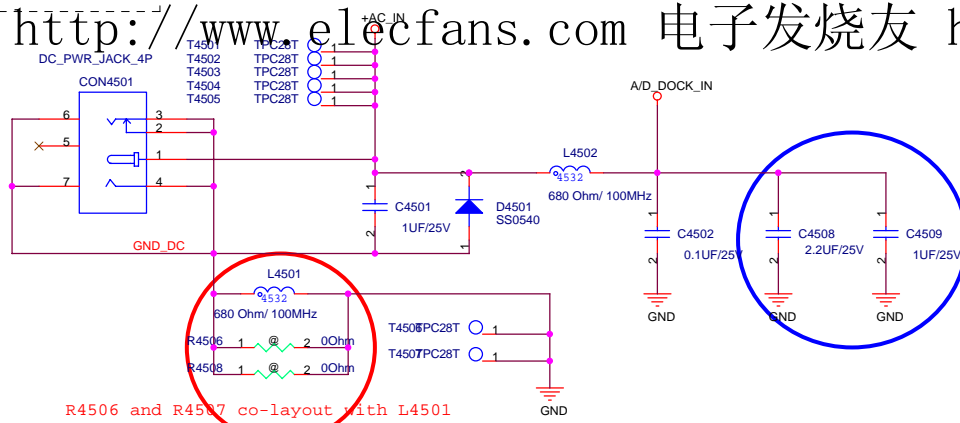




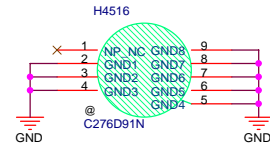
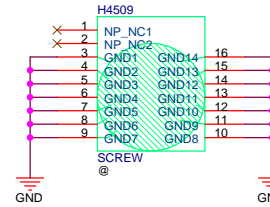
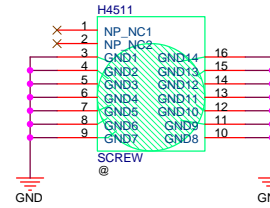
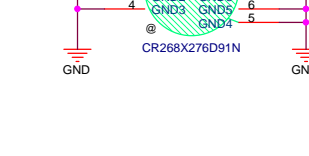
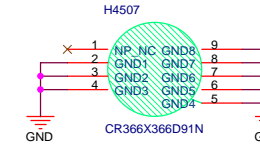
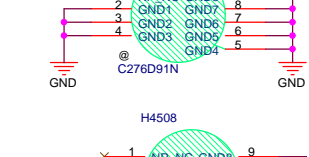
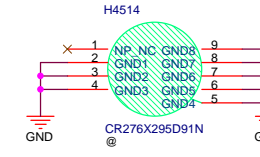
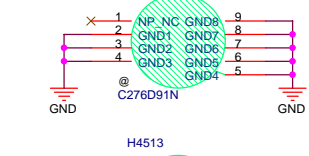
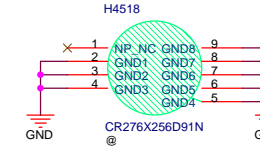
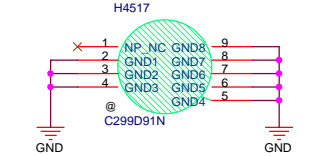
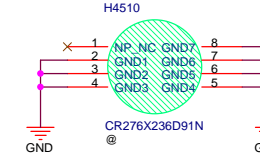
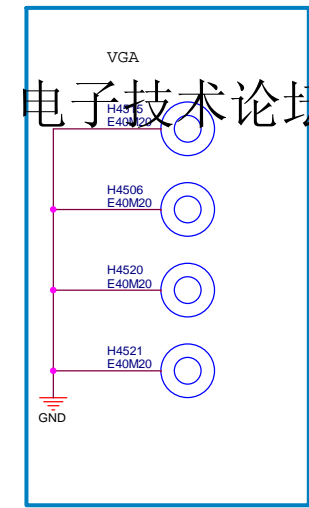
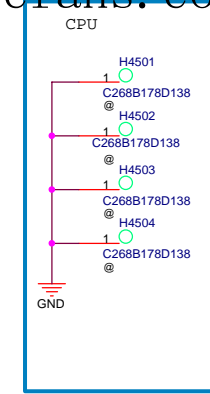
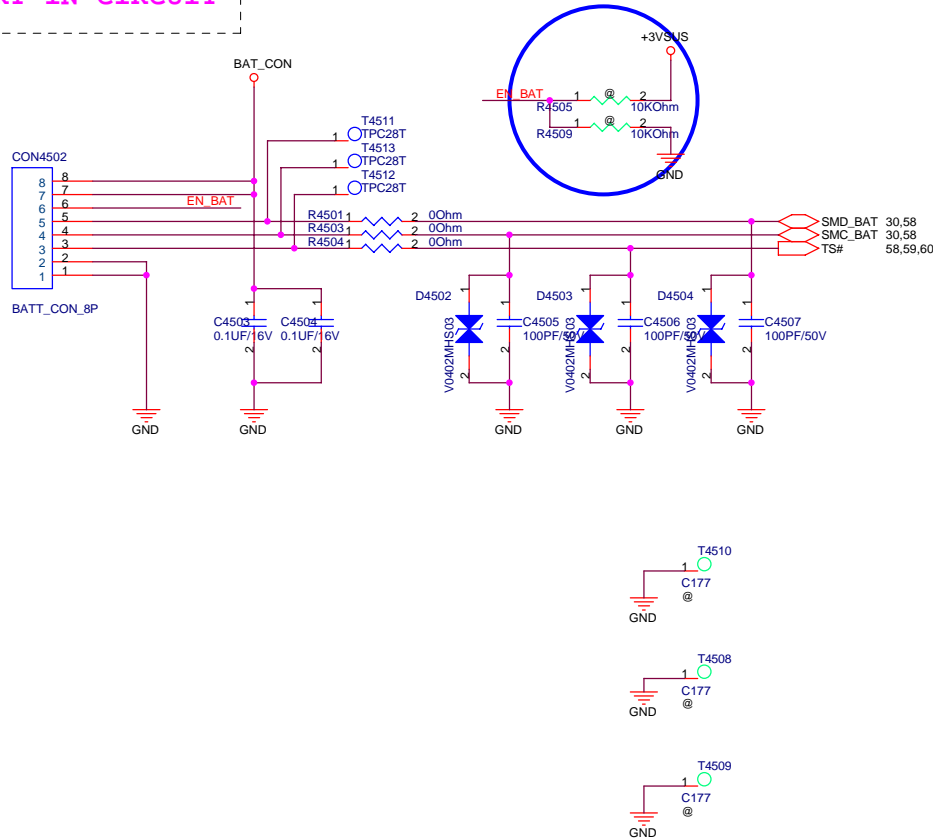
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ASUSTeK COMPUTER INC		Engineer: <u>Marco Chen</u>	
Size Custom	Project Name A6Jc		Rev 2.1
Date: <u>Thursday, January 19, 2006</u>	Sheet	<u>44</u>	of <u>63</u>

Adaptor IN Circuit

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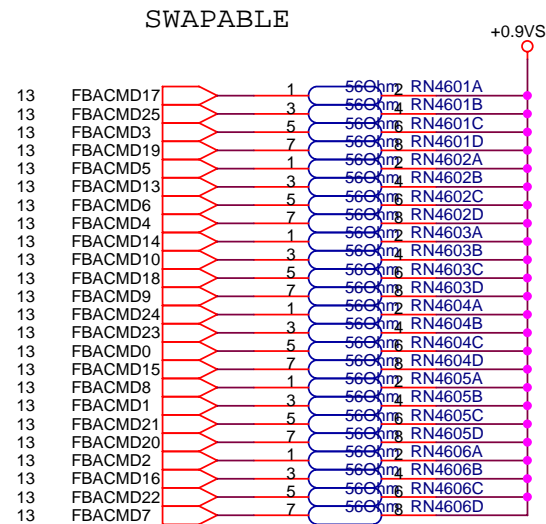
BATTERY IN CIRCUIT



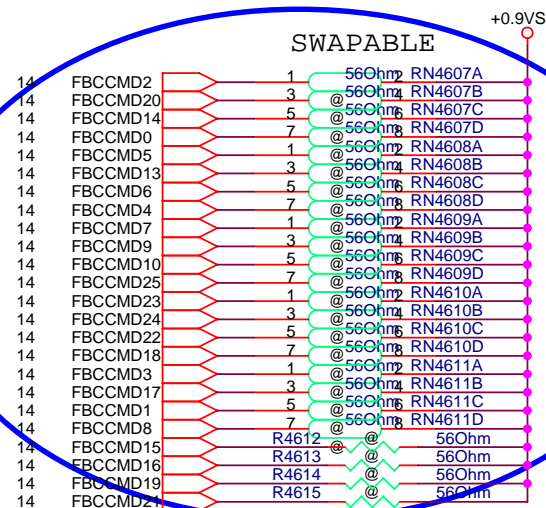
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ASUS		Title : Power Connector	
ASUSTeK COMPUTER INC		Engineer: Marco Chen	
Size	Project Name	Rev	
Custom	A6Jc	2.1	
Date: Thursday, January 19, 2006	Sheet	45	of 63

FBA CMD/ADDR Termination



FBC CMD/ADDR Termination



<Variant Name>

		Title : G73M-Termination	
<OrgName>		Engineer: Charles Lee	
Size	Project Name		Rev
Custom	A6Jc		2.1
Date: Thursday, January 19, 2006		Sheet	46 of 63

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Host	SM-Bus Device	SM-Bus Address	Device
ICH7-M	Clock Generator	1101001x (D2)	ICS954310
ICH7-M	SO-DIMM 0	1010000x (A0)	DDR SOCKET1
ICH7-M	SO-DIMM 1	1010001x (A4)	DDR SOCKET2
ICH7-M	Thermal Sensor	0101110x (5C)	ADT7463 (Optinal)

PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER	AD17	1	B
CARDBUS	AD17	1	C
1394	AD17	1	D

R1.0 -> R1.1

1. Page2: Add test points T215 and T216 for H_ADS# and H_CPURST#
2. Page4: Modify FAN Solution from DA to PWM and change R-C delay timing.
 - A. Mount R416 and DNI R415
 - B. Change C404 to 1uF
3. Page4: Connect +3VS_FAN(R419*3.3K ohm and R420*2.2K ohm 分壓 from +V5S_FAN) to U401.3 because FAN_DA level is 3V and FAN_PWM# is open-drain, change pull-up to +3VS and U401.3 level shift from 5V to 3V
4. Page4: Add pull-down resister R418*10M ohm to protect noise when power-on
5. Page5: Add (R579*33 ohm and C529*10pF) for TPM PCI 33MHz clock
6. Page5: Change R531 from 10 ohm to 22ohm to eliminate swing.
7. Page5: DNI R510 to disable ITP enable.
8. Page7: Delete R715 because it duplicate with R529.
9. Page9: Change L905 to P/N:09G012030000 and L905 to P/N:09G013120409 because +1.5VS_PCIE consume about 1.3A and +1.5VS_3GPLL consume 200mA only.
10. Page13: VGA_GPIOS add pull-up 10K ohm to +3VS for ATI recommendation.
11. Page13: DNI R1320 and mount R1321 to change back light enable from DC level to PWM and meet VBIOS support.
12. Page13: Add R1343*0 ohm for reserving bead to ground.
13. Page15: Change L1504.2 to connect from +VGA_VCORE to +1.2VSP for ATI recommendation.
14. Page15: Change bead L1506 from 120Ohm/100Mhz to 300Ohm/100Mhz type.
15. Page19: Add bead L1913 between TV_GND and GND.
16. Page23: Change High Definition damping resistors*R2312, R2314, R2316, R2318, R2320, R2322, R2324, R2325 from 22 ohm to 39 ohm for reducing reflection.
17. Page29: Add Line-in solution, please commt Black 2.
18. Page31, 32: Change LAN chip from Marvell 88E8053 to Realtek RTL8111B.
19. Page34: Add Q3401 and R3414 to replace U3402B.
20. Page34,35: Modify reset circuits to meet Intel specification, please commt Black 3.
21. Page35,43 : DNI R4312 and change R3509 from 4.7M ohm to 2.2 M ohm to short SWDJ_EN# detected to 2secends for BIOS requirement and add INIT# solution(please comment Block 7).
22. Page37: Change R3706 from 10K ohm to 100K ohm to enlarge R-C delay time.
23. Page39: Reserve R3905 to PLT_RSTNS# Wire-Or with PLT_RST#_BUF.
24. Page41: Short CON4101.1 and CON4101.2 and delete R4105, R4104, and C4103 because no timing issue between power and enable signal.
25. Page42: Delete D4201 and DNI R4202 because no power loss issue exist.
26. Page43: Modify S4 stretch circuits, please comment Block 4.
27. Page44: Add TPM connecter.
28. Page45: Add C4508, C4509, R4506 and R4507 for EMI requirment.
29. Page42: Change CON4202.1 and CON4202.3 power from +3VSUS to +3V.
30. Page18: Change L1806.2 power from AC_BAT_SYS to AC_BAT_SYS_CPU for EMI requirement.
31. Page7: Change from VRM_PWRGD to ICH7_PWROK to enable MCH_PWROK for Intel requirement(Mount R721 and DNI R722).

32. Page23,34: Change thermal-trip solution.

A. Mount R2315 and DNI R4507

B. Remove the diode (please comment Block 5)

C. Mount thermal protection circuits.(please comment Block 6)

33. Page5, 23, 37: Change capacitor values for TXC recommendations(C513,C514 from 33pF to 27pF, C2302, C2304 from 12pF to 22pF ,Change X3701 to 07G010S22450*30 ppm and C3725 and C3726 to 22pf).

34. Page15, 47: Add Back Bias circuits for ATI recommendations.

35. Page5, 23, 33: Add SATA circuits for OEM requirement.

36. Page12: Remove R1205 for ATI recommendations.

37. Page39: Reserve R-C to tune waveform quanlity.(R3906,R3907,C3911,C3912)

38. Page41: Reserve R4104, R4105, R4106 to modify enable blue tooth solution.

R1.1 -> R2.0

1. Page4, 34: Add power limit solution and change thermal protection solution.

A. Add R421*0 ohm and connect to H_PROCHOT_S#

B. DNI R417*0 ohm

C. Add R422*0 ohm and connect to OVERTEMP# that is wire-or with FORCE_OFF#.

D. DNI OTP solution.

2. Page15: Add BBIAS_CNTL pull-down resister R1508*10K ohm to GND.

3. Page19: Modify parts (D1912 and F1901).

4. Page24: Add 3 pcs decoupling CAPs(C2410, C2411, C2412) to short return path because PCI Bus(IN1) reference +1.8VS(Vcc).

5. Page25, 44: Add BT_LED solution to co-layout with Scroll Lock for Epson requirement.

6. Page27: Change R2704 from 0 ohm to 150 ohm.

7. Page27: Change R2707 from 47K ohm to 332K ohm.

8. Page27, 28: Add MUTE_POP# solution for Epson requirements. Please comment PR BLOCK 1.

9. Page30: Add LID switch solution.

A. Change BAT_SEL# push-pull resister from +3V to GND.

B. DNI Q3002*2N7002.

10. Page31: Change LAN chip reset signal from PLT_RSTNS# to PCI_RST#. (Mount R3107 and DNI R3106).

11. Page35: Change KBCRSM solution to connect to PM_PWRBTN# directly, please comment PR BLOCK 2.

12. Page36: Change CARDBUS chip reset signal from PLT_RST#_BUF to PLT_RST#. (Mount R3618 and DNI R3617).

13. Page39: Add WLAN_LED# pull-high resister R3908*100K ohm to solve LED was lighted when miniCARD was un-plug in.

<Variant Name>

		Title : History (1)	
ASUSTeK COMPUTER INC		Engineer: Marco Chen	
Size	Project Name		Rev
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14. Page40: Remove L4003, L4005, L4007, L4008 for EMI requirement.

15. Page43: Mount R4301*100K ohm to avoid PWR_FW# is floating.

16. Page43: Mount R4327*10K ohm to fix DJ_LED light soon issue when power on.

VGA NV G72M-V R1.0 -> R1.1


- 1. Page15: Change R1507 from 121 ohm to 0 ohm and Remove R1511 for SSC 3.3V requirment.
- 2. Page13: Change VRAM CLK Terminators R1303, R1304 from 120 ohm to 100 ohm for NV recommendation.
- 3. Page14: Change VRAM CLK Terminators R1402, R1403 from 120 ohm to 100 ohm for NV recommendation.
- 4. Page16: Change DACX_RSET R1605, R1607 to 124 ohm and remove R1604, R1606 for NV recommendation.
- 5. Page17: Mount 3GIO_PADCFG R1720 and DNI R1721 for NV recommendation.
- 6. Page17: Change RN1701 from 4R8P 0603 to 4R8P 0402 for BOM issue
- 7. Page19: Change D1913 from LM385M3 to BAV99.
- 8. Page19: Change L1901, L1905, L1906 to 180NH.
- 9. Page43: DJ_LED# Pull high to +3V via R4327 10Kohm.
- 10. Page35: Add D3509 (DNI) in parallel to R3532 for C3506 discharge path.
- 11. Page34: Change U3404 RN5VD to CMOS Topology and R3402(DNI).
- 12. Page04: Change R420 from 22K ohm to 10K ohm and change R419 from 33K ohm to 20K ohm for Volt divide.
- 13. Page43 :DNI C4306.
- 14. Page05: Change R519,R546 from 1 ohm to 2.7 ohm.
- 15. Page27: Change CE2701 from 47uF to 22uF and rename to C2727.
- 16. Page32: Change CE3301, CE3302 from 47uF to 22uF and rename to C3314, C3315.
- 17. Page17: Add U3003, Q3008(DNI) for 4S1P Battery detected.
- 18. Page23: Change X2301 to PN:07G010303270.
- 19. Page31: Change X3101 to PN:07G010S22500 for cost issue.
- 20. Page37: Change con3701 footprint to "nb_pcmcia_84p_6hold_a3n_lf2" for factory issue.
- 21. Page45: Change H4506, H4515, H4520, H4521 footprint to "nb_smt_nut_e40m20_lf2" for factory issue.
- 22. Page43: WLAN_LED# Pull-high to +3VS via R4328.
- 23. Page29: Change U2902 to PN 06G010147010.
- 24. Page14: Add R1415 and DNI L1403 for NV recommendation.
- 25. Page28: Change R2832 from 10K to 100K and R2806(DNI).
- 26. Page27: Change R2704 from 0 ohm to 100ohm.
- 27. Page35: Change R3509 from 2.2M ohm to 1Mohm and C3504 change from 1uF to 4.7uF.
- 28. Page31: Change R3106 DNI and R3107 stuff .
- 29. Page27: Change R2707 from 47k ohm to 332K ohm.
- 30. Page43:Mount R4301
- 31. Page35: Modify KBCRSM Circuit.
- 32. Page30:Add D3003 and C3007.

VGA NV G72M-V R1.1 -> R2.0

- 1. Page19: Change L1901, L1905, L1906 to 09G013120409 120ohm/100MHz.
- 2. Page31: Change C3133,C3134 from 22PF to 27PF.
- 3. Page46: Change ChipResistor RN4607~RN4612 to Single Resistor R4607 ~ R4630.
- 4. Page45: Change C4509 from 10uF to 2.2uf.
- 5. Page19: Change R1910 from 33Kohm to 47Kohm for BOM reduction.
- 6. Page15: Change R1501 from 71.5ohm to 81.6ohm for BOM reduction.
- 7. Page25: Add R2550 ,R 2553, R2555 for BT_ON.
- 8. Page14: Mount R1414 for NV recommendation.

C2827	MLCC 2.2UF/10V(0603)Y5V+80-20%	-->	MLCC 2.2UF/6.3V(0603)X5R 10%
C3007	CAP 2.2UF/6.3V(0603) Y5V (225)	-->	MLCC 2.2UF/6.3V(0603)X5R 10%
C3503	MLCC 2.2UF/6.3V(0603)Y5V+80-20%	-->	MLCC 2.2UF/6.3V(0603)X5R 10%
C3506	MLCC 2.2UF/6.3V(0603)Y5V+80-20%	-->	MLCC 2.2UF/6.3V(0603)X5R 10%
C3502	MLCC 4.7UF/6.3V(0805) X5R 20%	-->	MLCC 4.7U/6.3V(0805) X7R 10%
C3405	MLCC 2.2UF/6.3V(0603)X5R 10%		不變
C3411	MLCC 0.22UF/10V(0603)X7R 10%		不變
C3504	MLCC 4.7UF/6.3V(0603)X5R 10%		不變

<Variant Name>



Title : History(2)

<OrgName>

Engineer: Marco Chen

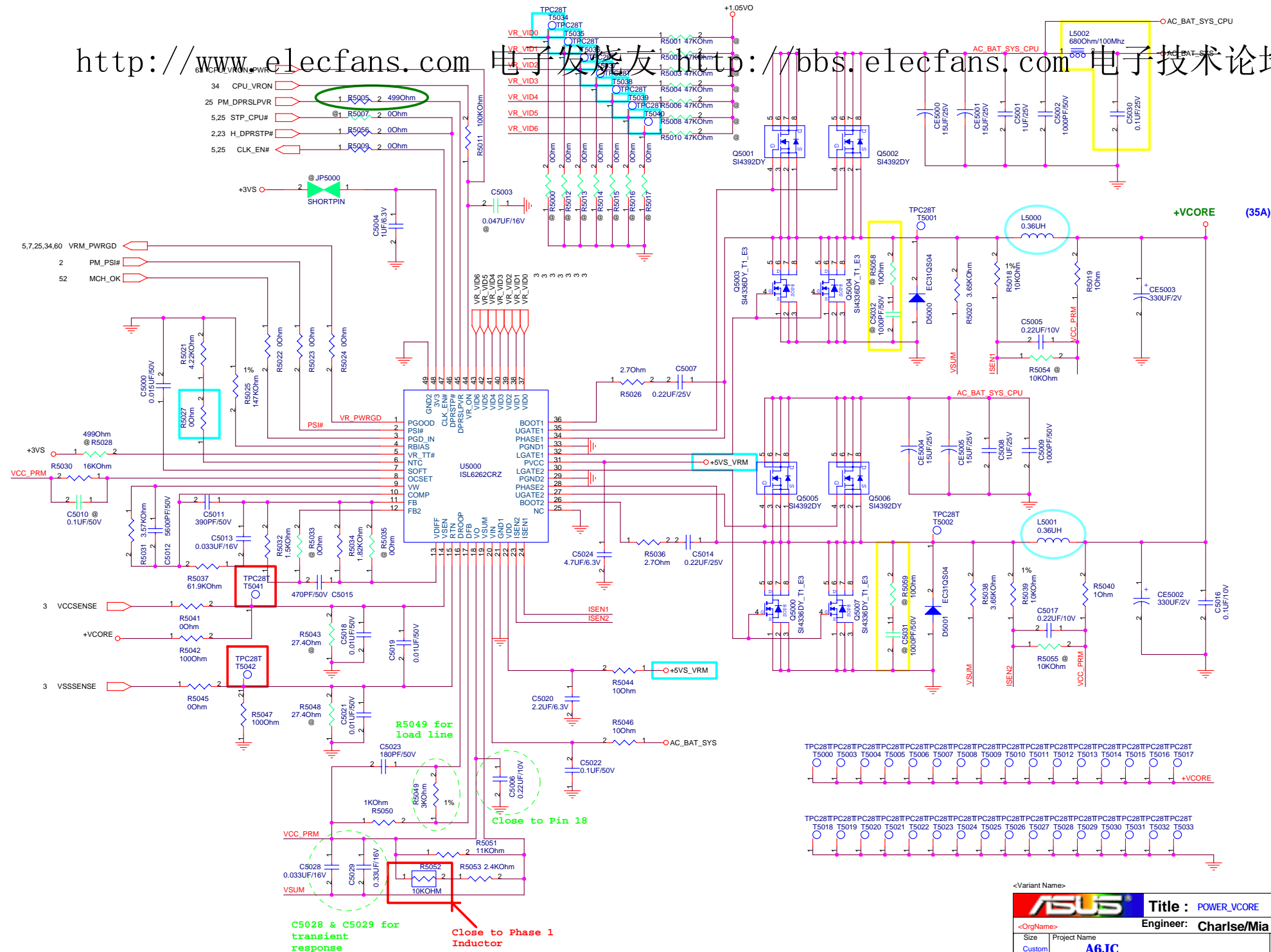
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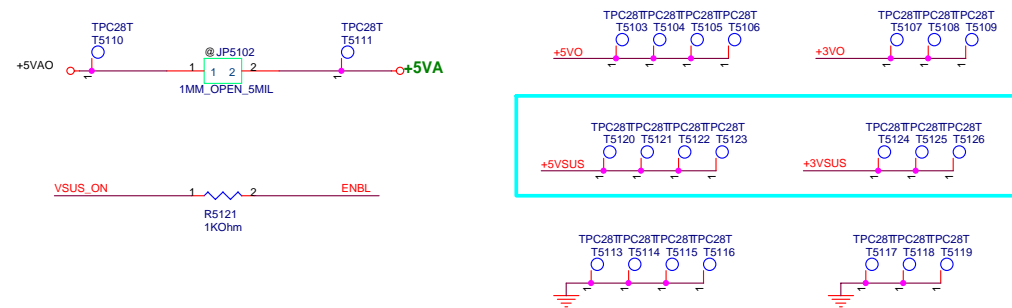
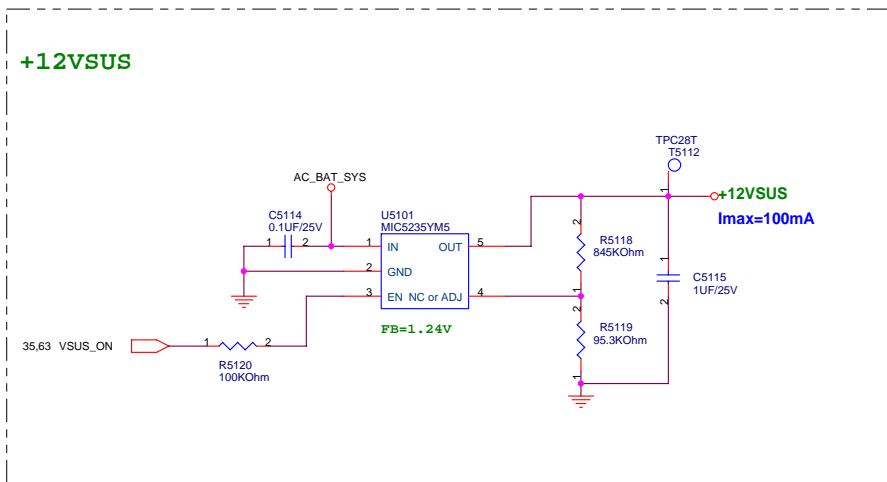
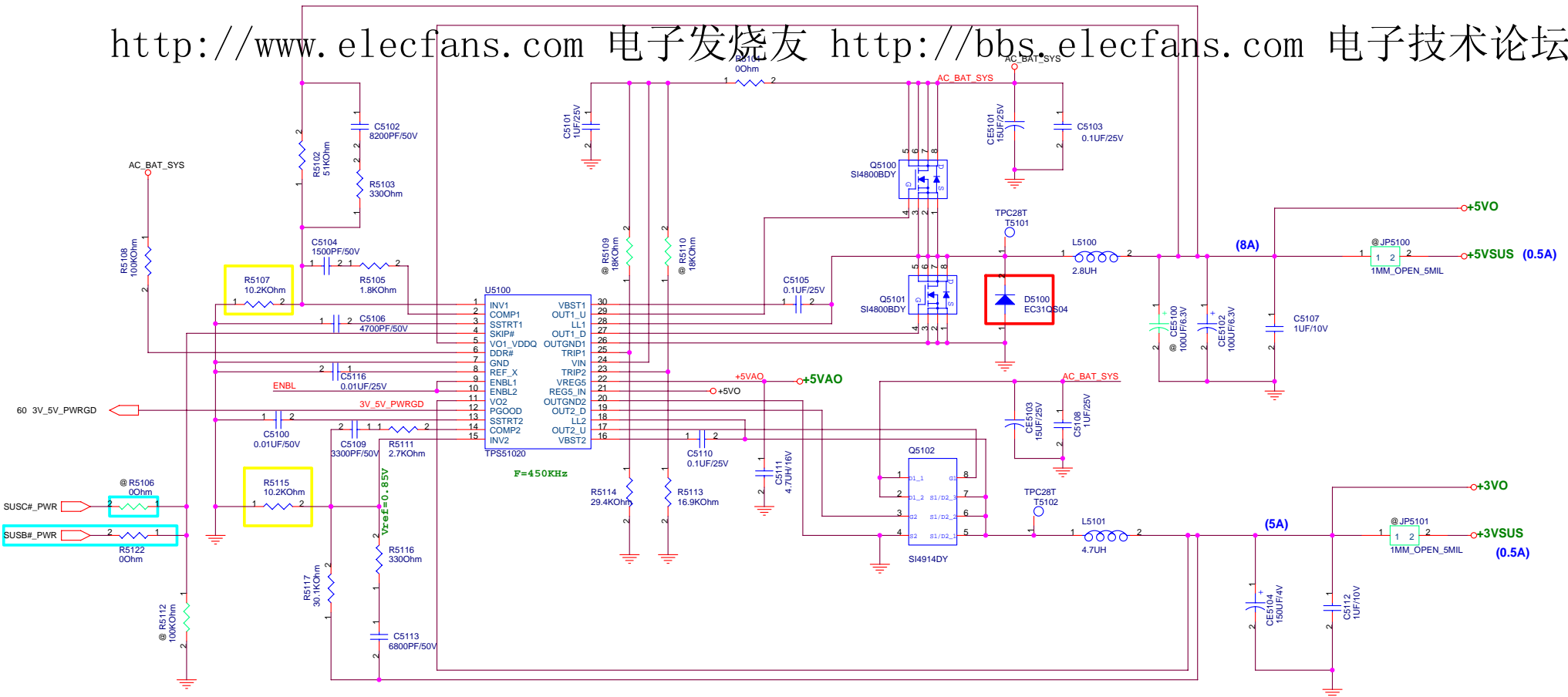
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A6Jc

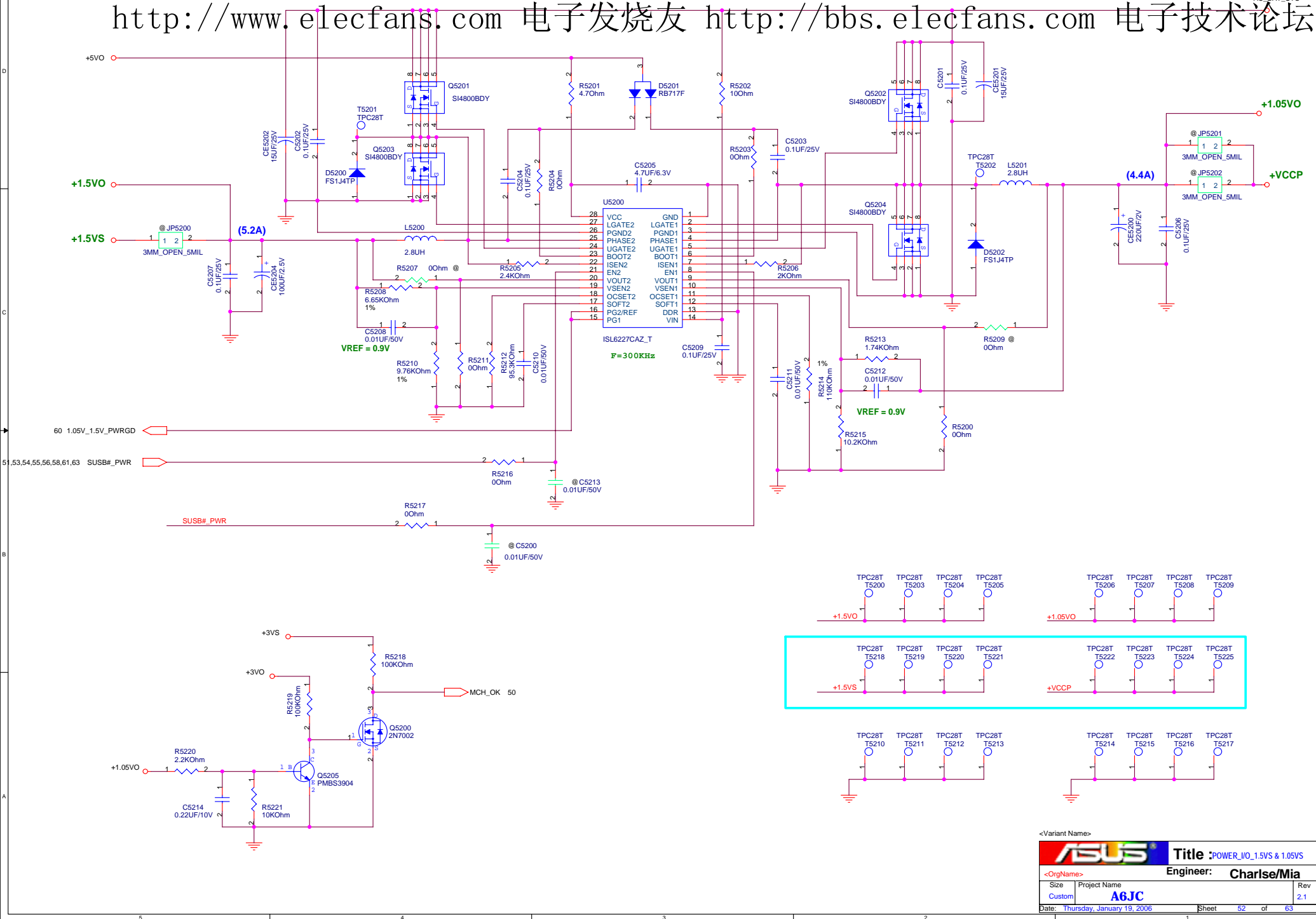
Rev
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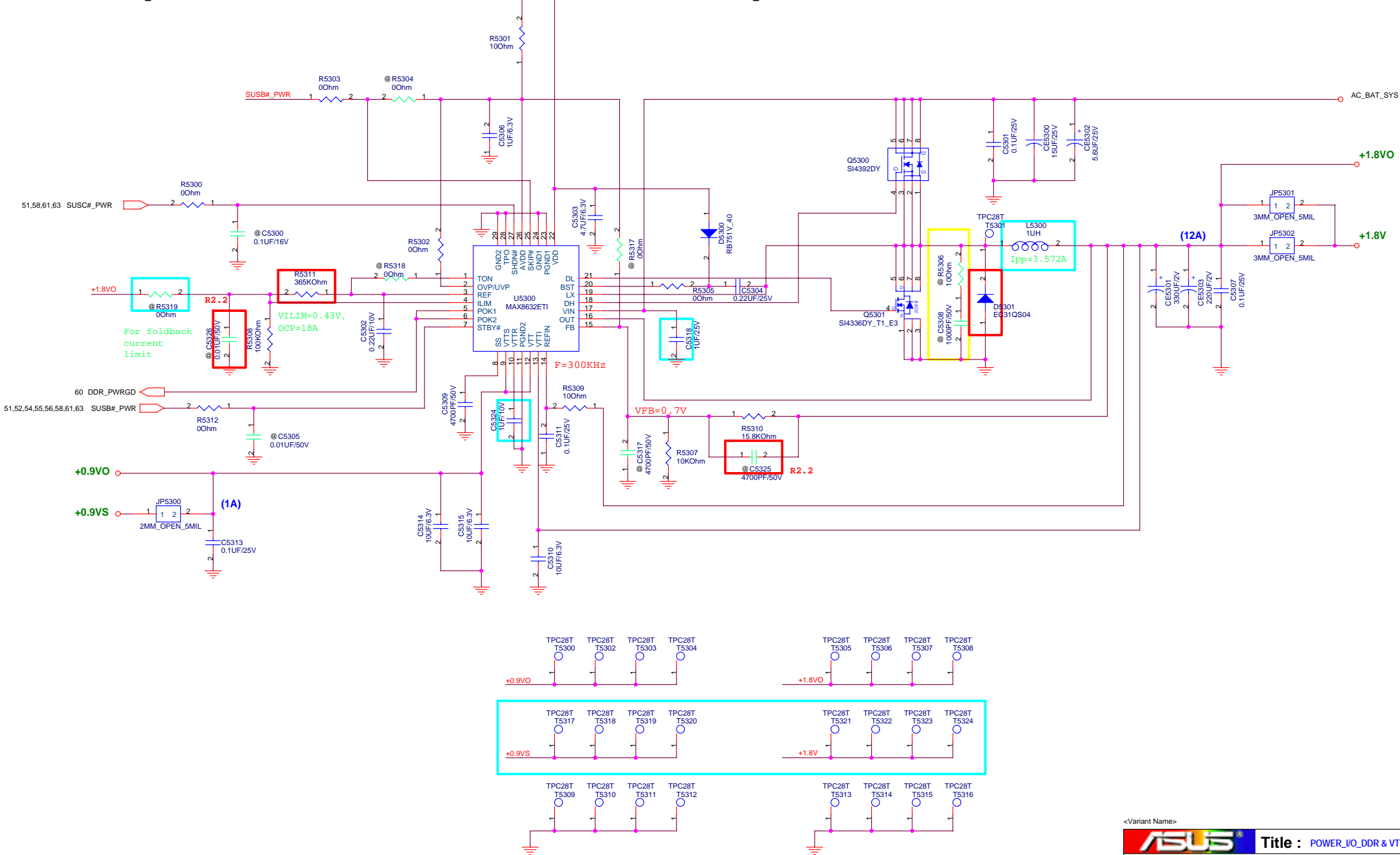
Date: Thursday, January 19, 2006

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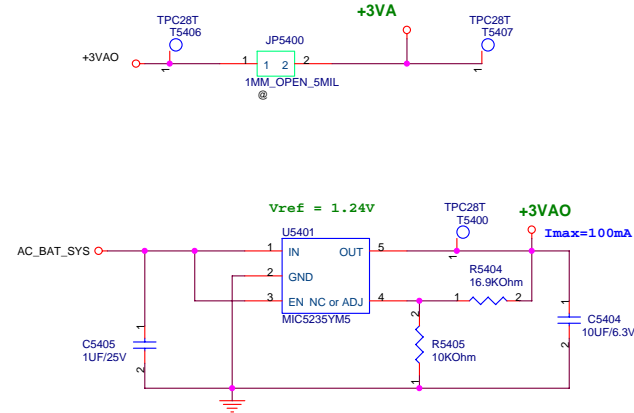




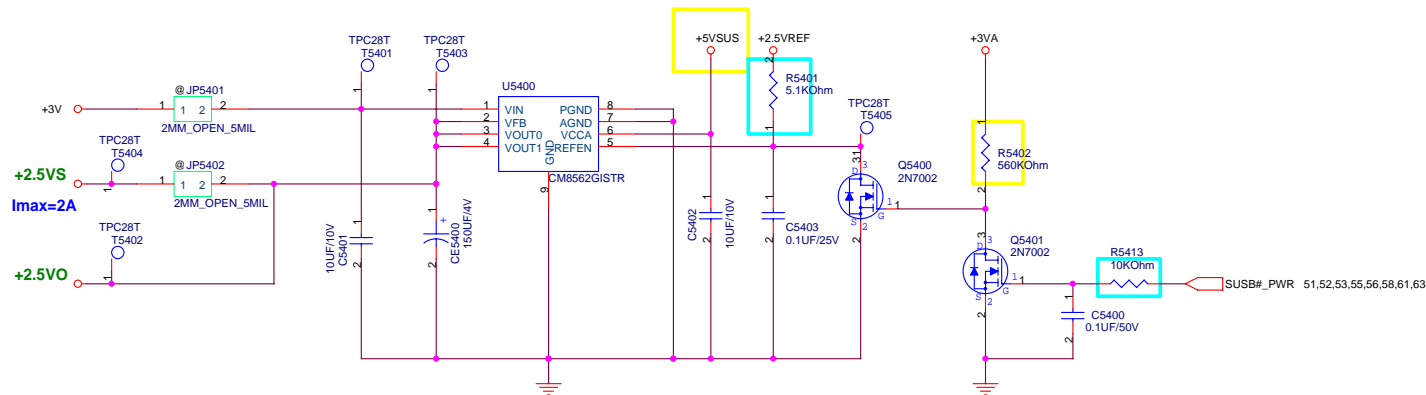




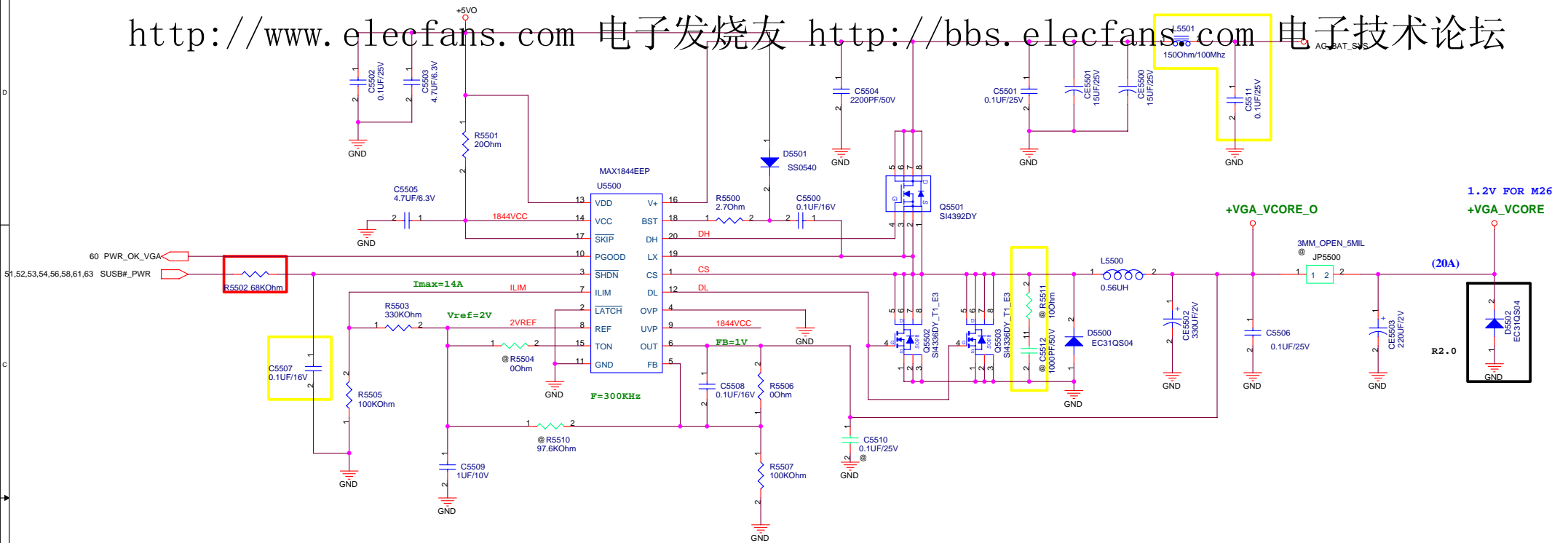
+3VAO



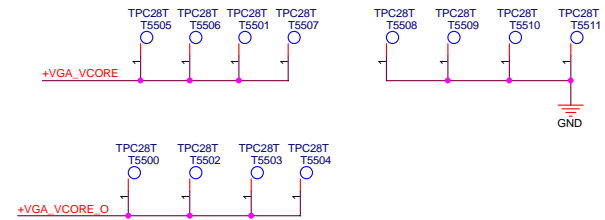
+2.5VS



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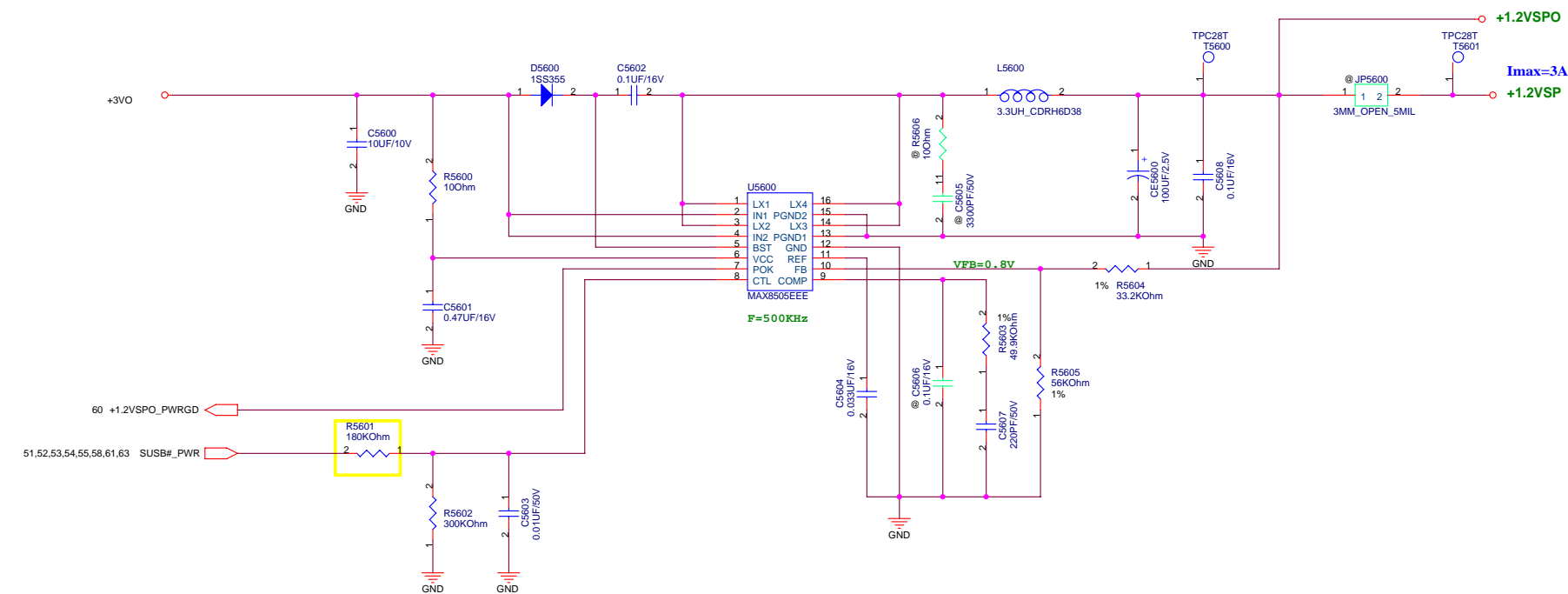


Model	VGA	+VGA_CORE	R5506	R5507	R5510
A6JC	G72M-V	1.0V	0	100K	@
A6JM	G73M	1.1V	10K	100K	@



<Variant Name>

ASUS		Title : +VGA_CORE	
<OrgName>		Engineer: Charlse/Mia	
Size	Project Name	Rev	
Custom	A6JC	2.1	
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<Variant Name>



Title : POWER_VGA_+1.2VSP

<OrgName>

Engineer: CharlseMia

Size
Custom

Project Name
A6JC

Rev
2.1

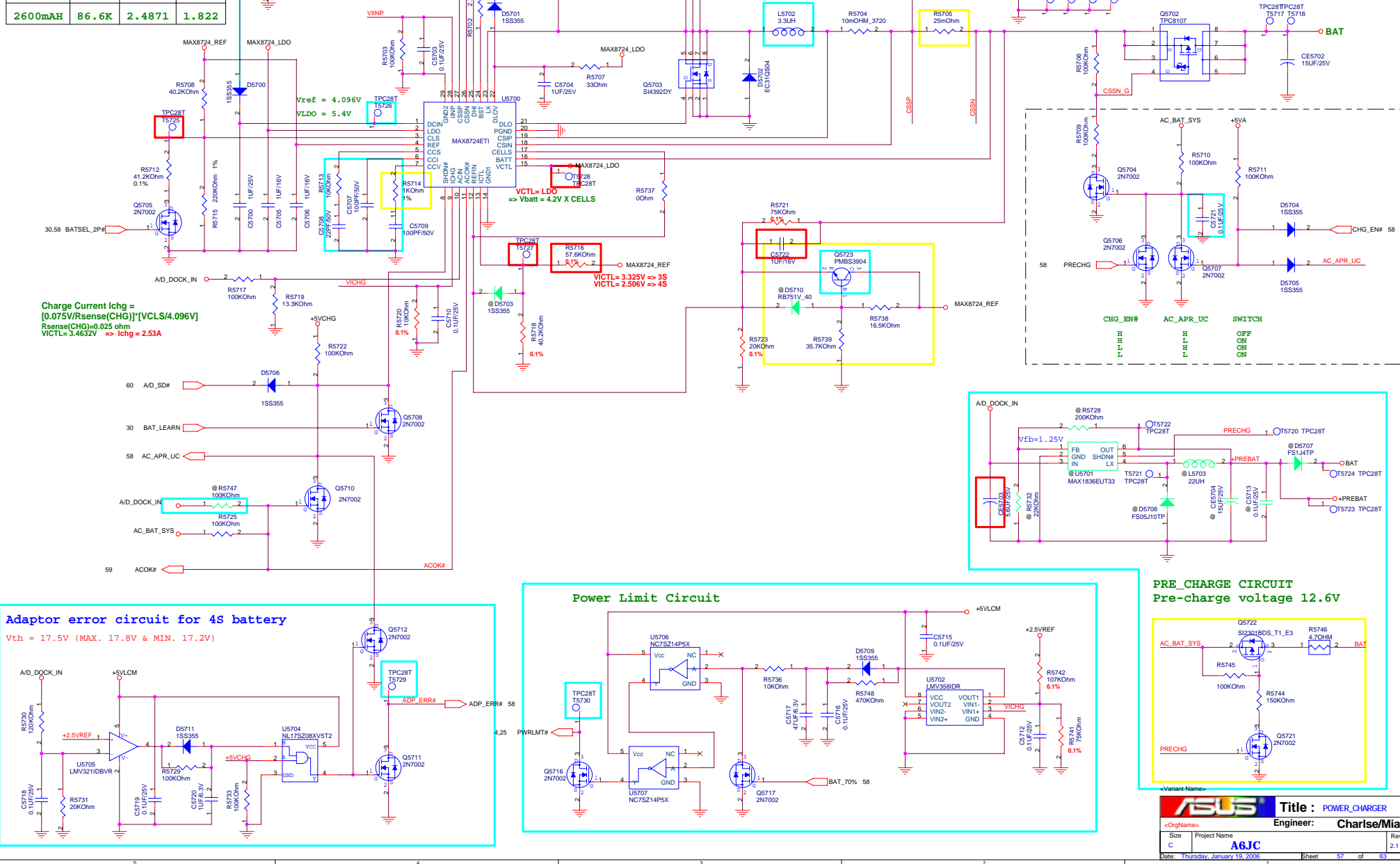
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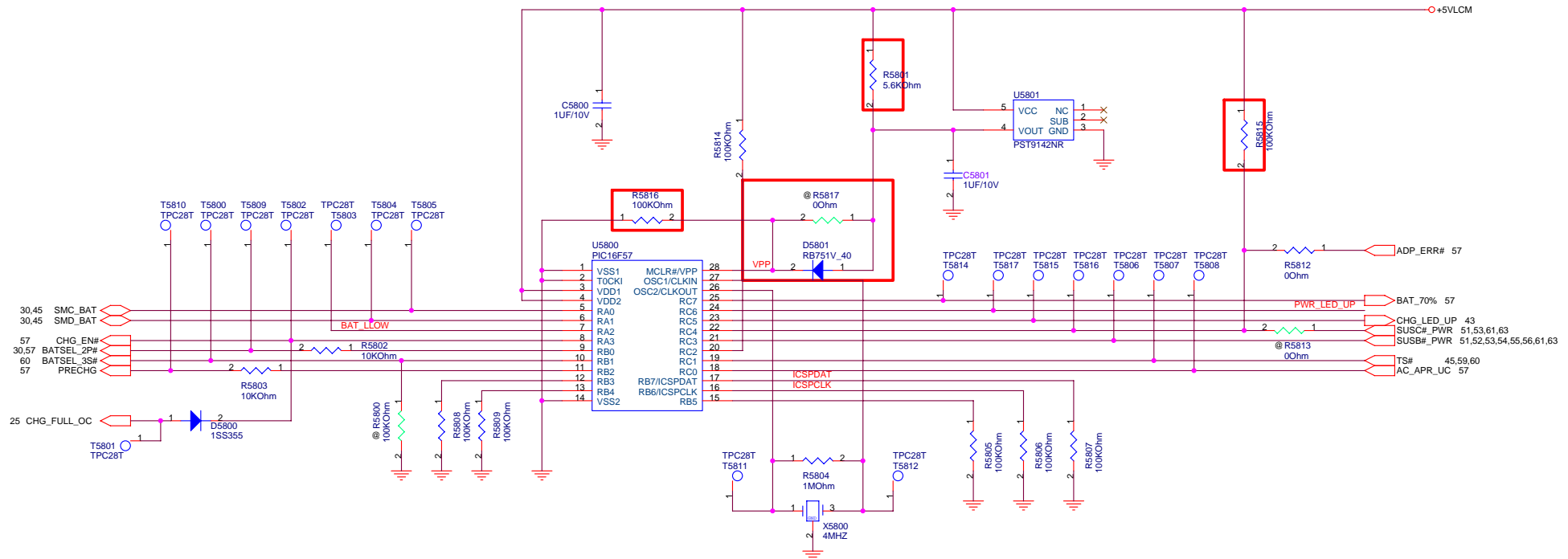
http://www.elecfans.com 电子发烧友 http://bbs.elecfans.com 电子技术论坛

BATSEL_2P# = "H" (1P)			
BAT capacity	R5712	VICTL(V)	ICHG(A)
2000mAh	41.2K	1.8976	1.39
2200mAh	52.3K	2.0989	1.537
2400mAh	66.5K	2.2918	1.679
2600mAh	86.6K	2.4871	1.822

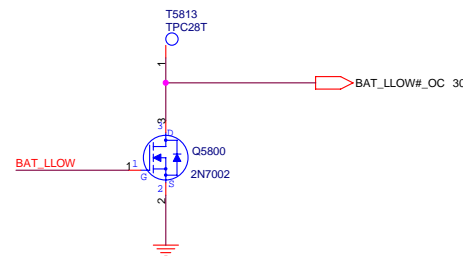
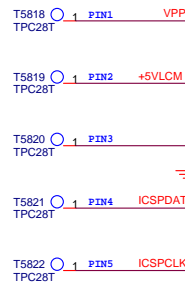


PIC16F57

<http://www.elecfans.com> 电子发烧友 <http://bbs.elecfans.com> 电子技术论坛



For PIC refresh



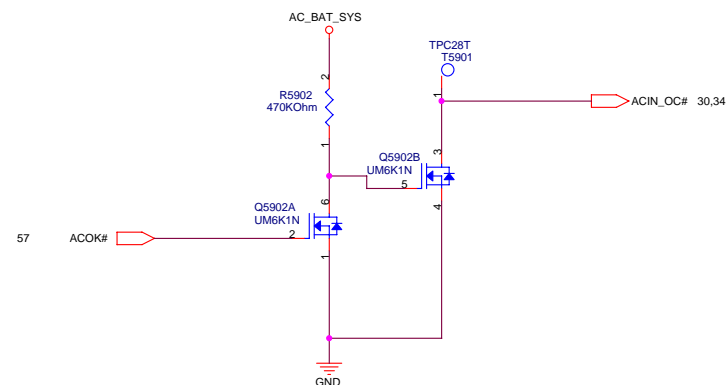
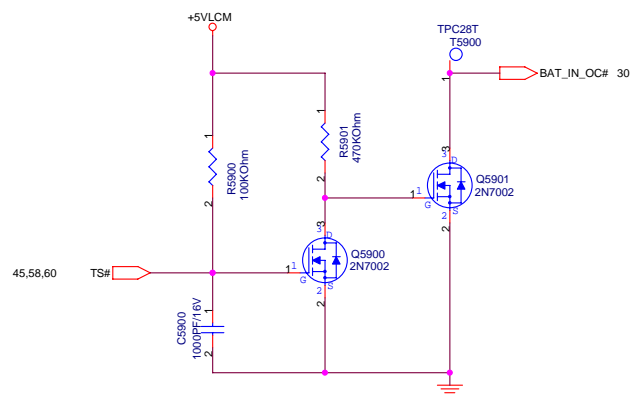
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Size	Project Name	A6JC	Rev 2.1
Custom			
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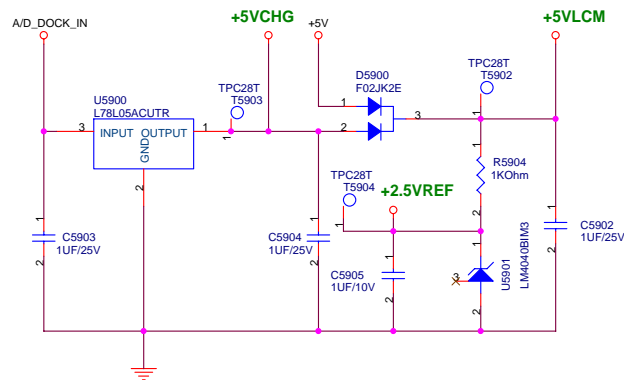
BATTERY IN DETECT

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ADAPTER IN DETECT



+5VLCM, +5VCHG & +2.5VREF



<Variant Name>



Title : POWER_DETECT

<OrgName>

Engineer: Charlse/Mia

Size

Custom

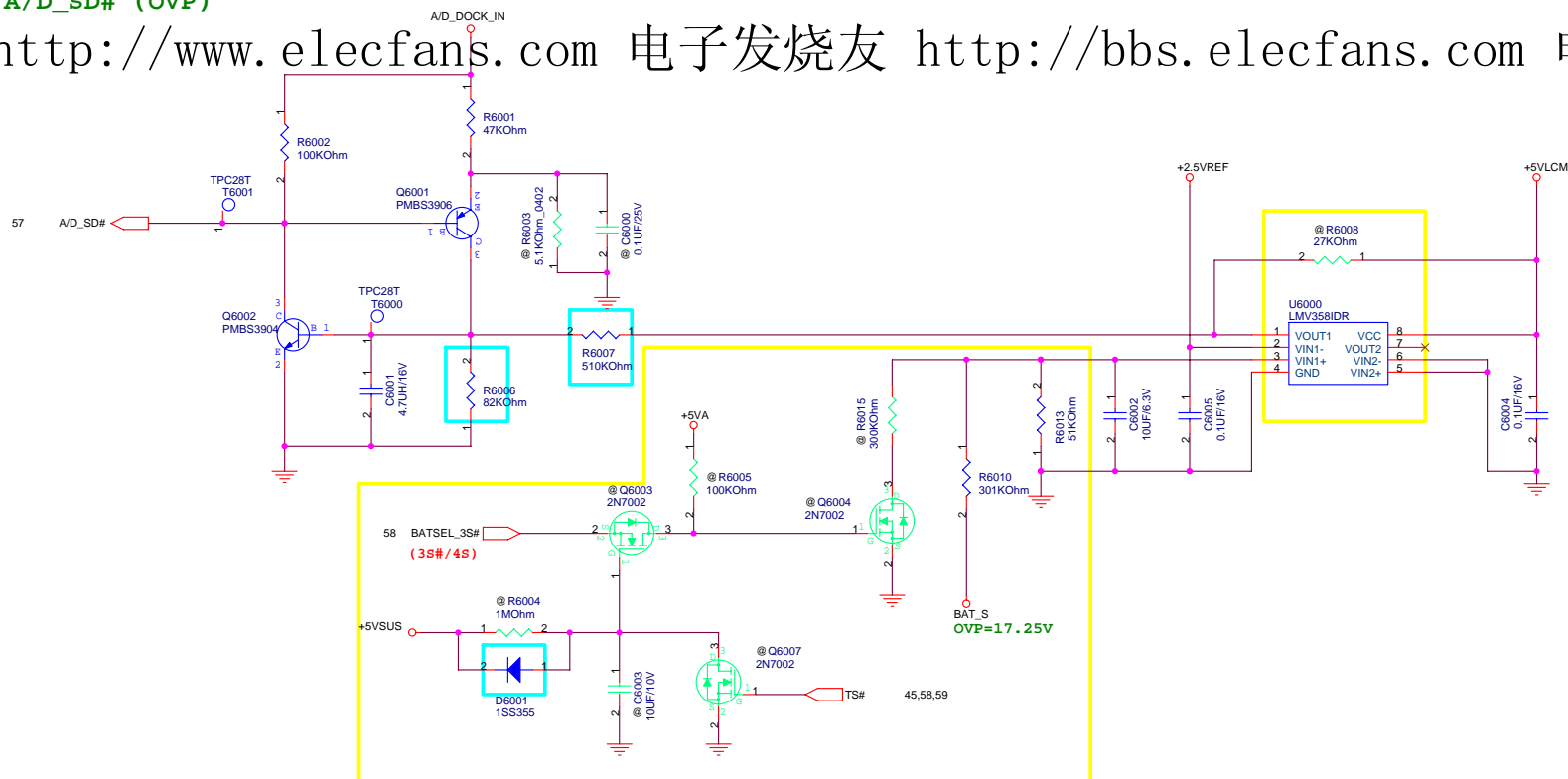
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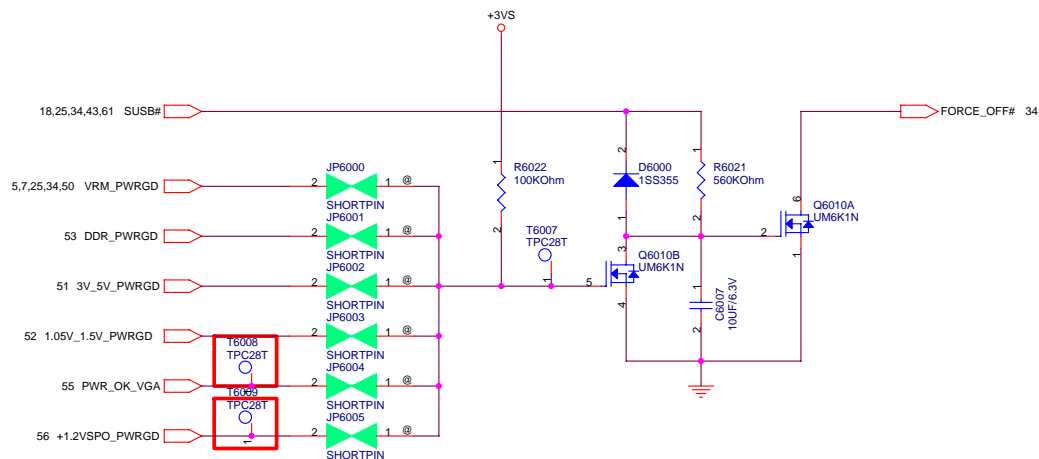
Rev 2.1


BATTERY A/D_SD# (OVP)


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POWER GOOD DETECTOR



TPC28T T6002  1 VRM_PWRGD

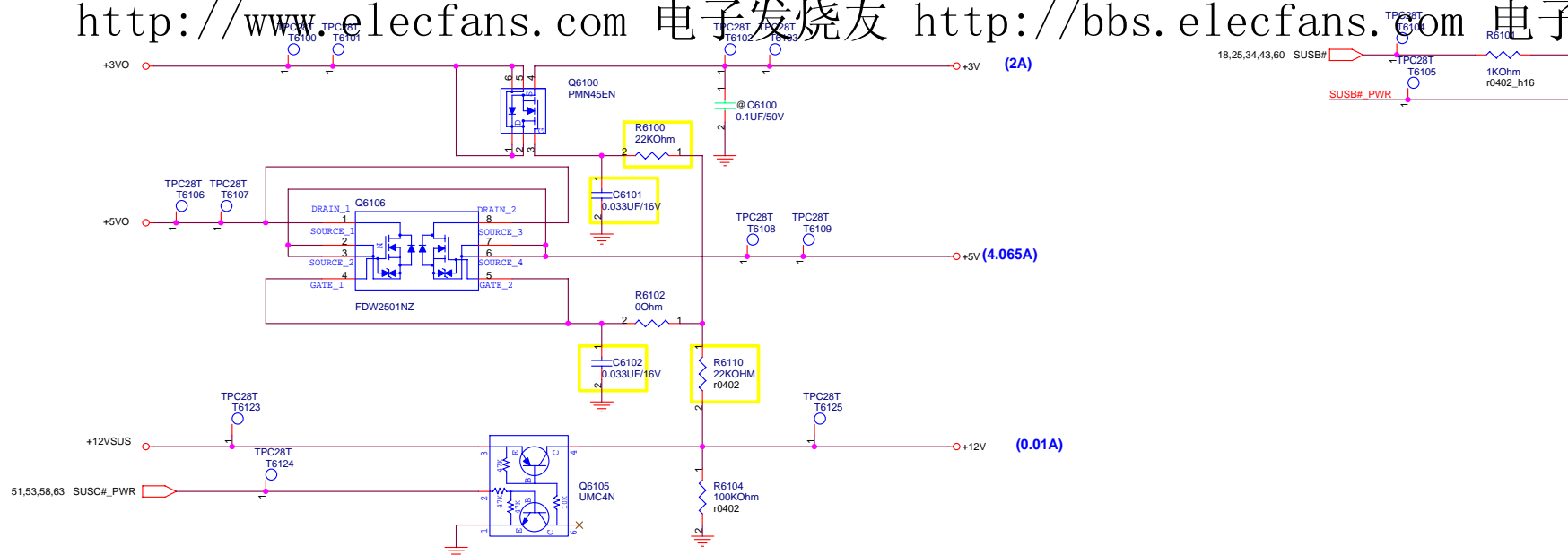
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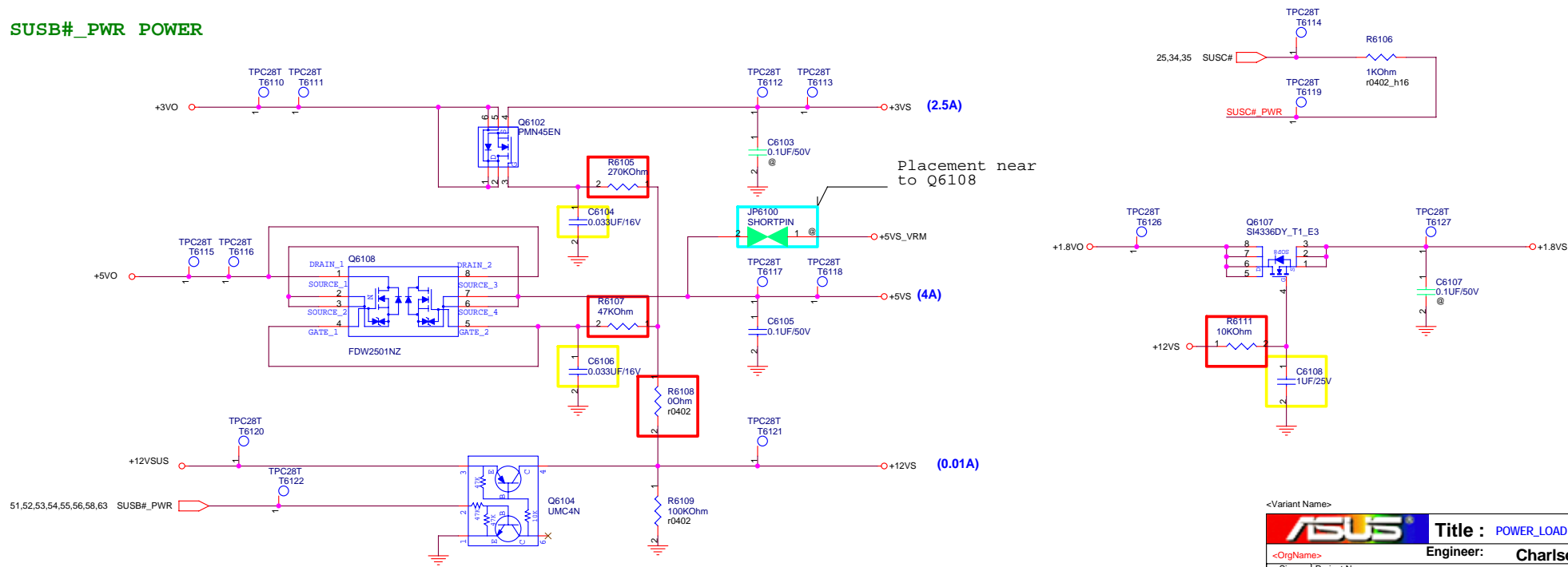
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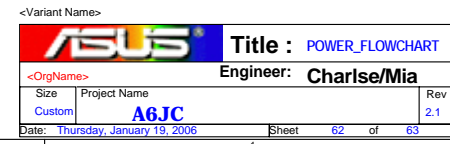
SUSC#_PWR POWER

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SUSB#_PWR POWER





AC_BAT_SYS ○ → AC_BAT_SYS 50,51,52,53,54,55,57,59
+3VA ○ → +3VA 18,23,34,35,43,54
+5VA ○ → +5VA 34,51,57,60
+5VO ○ → +5VO 51,52,53,55,61
+3VO ○ → +3VO 51,52,56,61

+3V ○ → +3V 25,30,31,32,35,36,37,38,41,42,43,44,54,61
+3VS ○ → +3VS 4,5,7,9,11,12,16,17,18,19,20,21,25,26,27,28,30,31,33,34,35,36,39,42,43,44,50,52,60,61

+12VSUS ○ → +12VSUS 51,61
+12V ○ → +12V 4,28,35,40,43,61
+12VS ○ → +12VS 18,19,35,61

+5V ○ → +5V 18,30,35,37,40,43,59,61
+5VS ○ → +5VS 4,19,22,26,27,30,33,35,41,43,61

+2.5VO ○ → +2.5VO 54
+2.5VS ○ → +2.5VS 9,15,16,19,35,54
+1.8VO ○ → +1.8VO 53,61
+1.8V ○ → +1.8V 7,10,20,21,35,53
+1.8VS ○ → +1.8VS 13,14,15,16,22,35,61

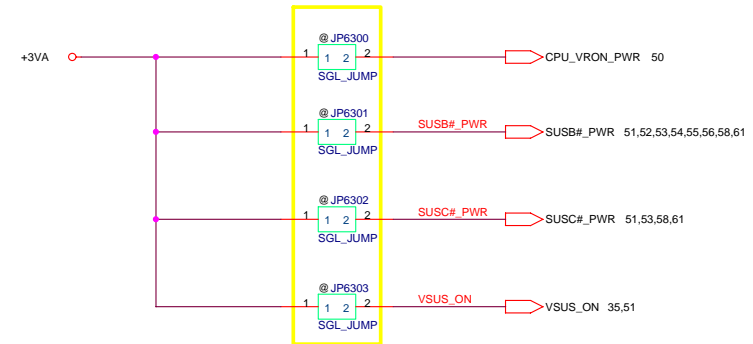
+0.9VS ○ → +0.9VS 14,15,22,35,46,53
BAT ○ → BAT 57
+5VCHG ○ → +5VCHG 57,59
+5VLCM ○ → +5VLCM 30,43,57,58,59,60
+2.5VREF ○ → +2.5VREF 54,57,59,60
+VCORE ○ → +VCORE 3,4,50

+VGA_VCORE ○ → +VGA_VCORE 12,55

+1.2VSP ○ → +1.2VSP 12,13,14,35,56

BAT_CON ○ → BAT_CON 45,57

FOR POWER TEST



<Variant Name>



Title : POWER_SIGNAL

<OrgName>

Engineer: Charlse/Mia

Size
Custom

Project Name
A6JC

Rev
2.1

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